SAMPLING AND CODING AS A MEANS OF REDUCING TIME AND AMPLITUDE DISTORTION IN RECORDING

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ABSTRACT

Time and amplitude distortion are present in both the record and playback processes in recording. This thesis investigates a means of eliminating this distortion when using magnetic tape by recording the information as groups of pulses which represent periodic digital samples of the desired waveform. In less general terms, the object is to take a waveform assumed free of distortion, sample it periodically, encode the samples in digital form in a binary system, and simultaneously record all the digits and a clock pulse on a multi-channel tape. For playback, all the digits will be selected by groups in the proper sequence at regular intervals determined by another clock independent of the recorder. These digits will be decoded and filtered to restore the original information. Errors will be functions of the coding and decoding processes, and will be independent of flutter, wow, and amplitude distortion in the tape.

A method was developed for selecting the digit groups in the proper sequence at regular intervals. In actual operation one of the individual selector sections did not perform properly, which prevented the system from achieving the desired over-all operation.

It was concluded that the method devised is both feasible and practical, although for high sampling rates an improvement in pulse recording techniques is required.

Secondly, it was determined that any such method requires an auxiliary servomechanism to compensate for long-term errors (e.g. stretch in the tape).

Thesis Supervisor: Richard H. Bolt
Title: Professor of Acoustics

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I. INTRODUCTION

The primary purpose of this thesis is to determine a means for reducing the time and amplitude distortion associated with the recording and playback processes when time-varying information is stored on any recording device. In the analysis of information which has been recorded, these errors limit the degree of precision possible and can result in losing the original information altogether.

Time distortion arises when equal intervals of time in the original information are reproduced at unequal intervals.

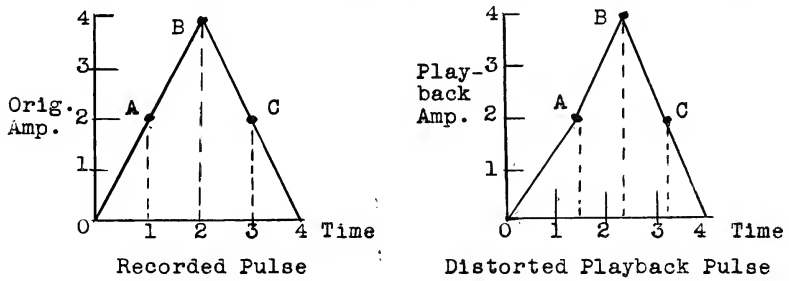
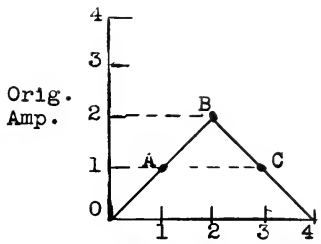


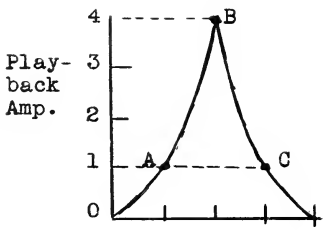
Figure I - Time Distortion

Figure I shows the unequal intervals which can result from time distortion. It should be noted that the amplitudes have not changed but that the time axis is distorted, thus distorting the entire waveform.

Amplitude distortion arises when the amplitudes of the reproduced information are not all directly and exactly proportional to the amplitudes of the original information.



Recorded Pulse



Distorted Playback Pulse

Figure II - Amplitude Distortion

Figure II shows such distortion. It should be noted that the time intervals are equal but that the amplitudes follow (in this case) a square law.

In actual recording systems, time distortion takes the form of wow and flutter. Wow is a low frequency speed variation of the playback mechanism such as would be caused by an eccentric phonograph record. Flutter is a high frequency speed variation such as would be caused by a flat spot on a phonograph motor drive shaft or on a tape drive capstan in a tape system. Flutter and wow can also be caused by vibration of transducers.[2]

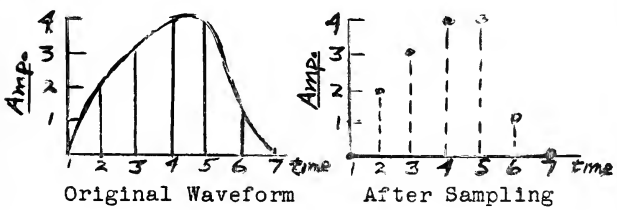
Amplitude distortion is introduced into recording by non-linearity at any point in the process. There are amplifiers and transducers, and the medium itself, all of which are subject to amplitude distortion.

Modern high-fidelity equipment reduces time and amplitude distortion by brute-force methods. Heavy moving parts have the inertia to keep vibrations down, and close machinery tolerances prevent flat spots and backlash. Synchronous

motors assure constant-speed drive. Nevertheless, wow and flutter are still present. Amplitude distortion is reduced by high quality amplifiers and a high frequency "bias" or magnetic dither superimposed on the recording signal. These methods do not achieve perfection either where precise amplitude information is required.

This thesis investigates an entirely different method of eliminating these distortions. The method is to record the information in the form of samples*, which will be taken sufficiently often to contain all the information. These samples will be recorded in digital form as pulses in a multi-channel recording system.

Sampling is the process of taking a sufficient number of points on a curve to define the entire curve. Figure III shows a waveform before and after sampling, and Table I shows the sampled values.



Original Waveform After Sampling

Sample No.	Amp. Binary Digits
1	0
2	10
3	11
4	100
5	100
6	01
7	0

Figure III - Sampling Table I - Samples

There are certain advantages to this system of recording. First of all, it is a digital system which operates on the

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*Appendix A describes the mathematics of sampling.

presence or absence of pulses, and is not subject to errors caused by amplitude distortion while the information is in digital form. Of course, there are problems associated with the conversion of the information to digital form, but converters are available commercially and the problems have been solved. The point is that it would be the converters that would introduce any amplitude distortion, and not the recording system with this method.

The second great advantage of sampling is that each sample is identified with a particular instant of time. It is therefore possible to reproduce each sample at a particular instant of time. This would thus eliminate any time distortion which might be present.

There are also obvious disadvantages to a sampling and coding system of recording. First, sampling imposes a frequency limitation on the sampled information and a bandwidth requirement on the electronic apparatus. Second, the multi-channel recording leads to large and expensive apparatus.

Sampling has been tried before. A thesis by Hitt [1] investigates recording samples as pulses of varying duration on a single channel. One of the limitations was the difficulty of storing the analog information contained in the samples. Also, the pulse interval must be longer than the longest pulse, so there is an upper frequency limit on such a system.

The system proposed in this thesis is shown in a

functional block diagram in Figure IV. The information to be recorded is put into a coder. A periodic clock input causes the coder to sample and encode the information in a digital system. The output of the coder then triggers pulse generators which supply the inputs to drivers of the record windings of a magnetic tape recording system. A periodic "marker" pulse is recorded along with the digit pulses in order that the groups of digits may be identified conveniently later. Thus the information is stored as periodic binary digital samples on the magnetic tape.

For playback the pulses which now have time distortion introduced by the recording system are first amplified and then stored in a Variable Delay Memory Unit. The average delay is such that there is a backlog of several groups of digits in the memory. A perfectly regular clock pulse then picks out the groups of digits in sequence and causes them to trigger the Read-Out Pulse Generators. The read-out pulses are decoded by the Decoder. The output of the Decoder requires only passive filtering to restore the original information, without time or amplitude distortion.

Such a system as this naturally requires components capable of performing the desired functions. There are, however, certain specifications which are implicit in this method.

The coder in the recording system and the decoder in the playback system must be able to perform their respective functions at the sampling rate required for the information

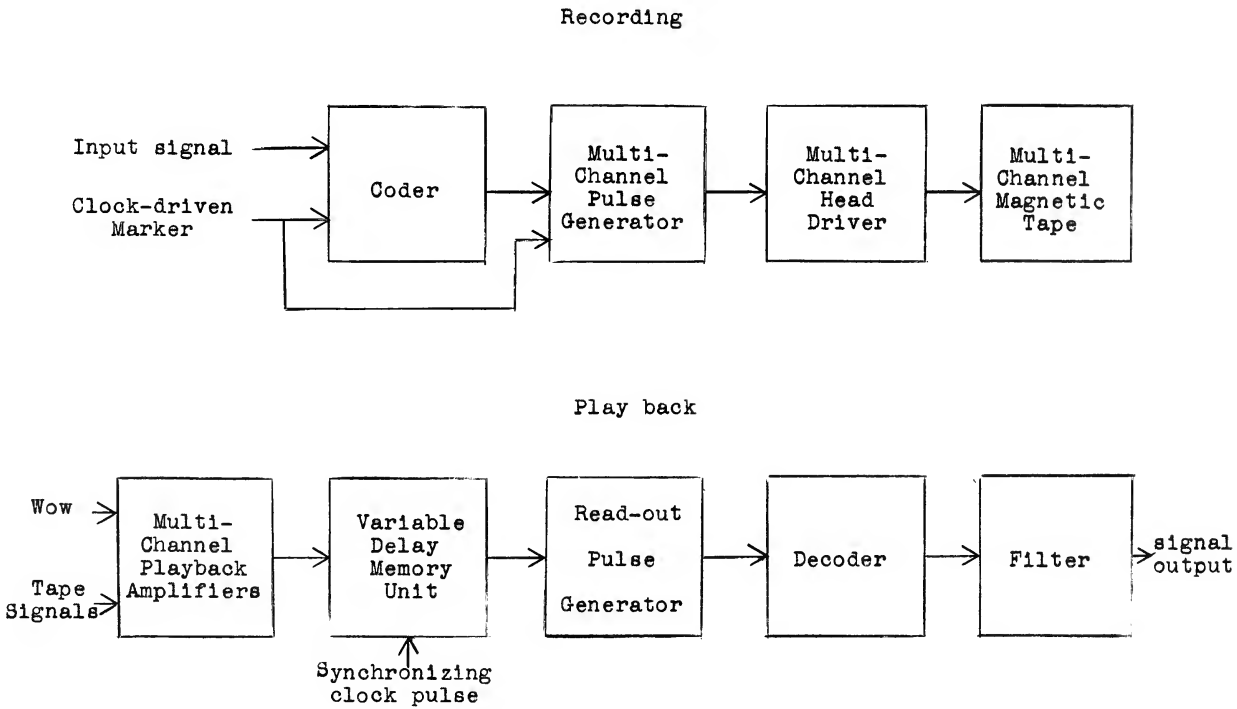

Figure IV

Elementary Block Diagram of System

recorded.

The sub-system consisting of record pulse generators, head drivers, record heads, tape, playback heads, and playback amplifiers must be capable of recording and reproducing the pulses at the sampling rate. However, it is only necessary that the reproduced pulses be detectable and unambiguous. They need not be similar to the recorded pulses.

The variable delay memory unit must have sufficient maximum delay available to store information which arrives too early, and it must have sufficient average delay to ensure always having information stored when the arriving information is too late. Thus, its capacity is a direct function of the time or position error of the tape transport system.

The read-out pulse generator is simply a matching device to make the output of the memory system suitable for operating the decoder.

The output filter must be designed to separate the desired information from the analog samples put out by the decoder.

The primary nature of this thesis, then, is to determine the numerical specifications for, and limitations on, the equipment between coder and decoder, and with the development of detailed designs for the equipment itself.

II. PROCEDURE

A. Preliminary Considerations

This thesis proceeded concurrently along two paths. One was the development of the variable delay memory unit with regard to the ultimate performance desired, but without considering the limitations of the tape recorder actually available. The other path was the determination of the characteristics of the actual recorder and the development of techniques for recording and reproducing pulses with the recorder. This approach was justified since magnetic tape recorders vary greatly in their characteristics and are still subject to much improvement. Because of this the parts external to the basic recorder should not limit the overall system.

B. Variable Delay Memory Unit

The variable delay memory unit is a system for storing groups of digits when received and releasing them when called for by a periodic clock. The storage means may be electronic flip-flops, magnetic memory units, or any other bi-stable or poly-stable device. It was decided that a simple magnetic memory would be suitable, especially since it is quite insensitive to noise and consumes no power while idling. This decision means that part of the system must deal in binary digits.

The use of binary digits has already been tacitly accepted in the introduction. The relation between the desired amplitude accuracy and the number of digits per

sample is therefore specified*. Since some commercially available coders use eleven binary digits and are capable of amplitude accuracies of ± 0.1% of the maximum amplitude, the system should be capable of processing at least eleven tape channels to retain this degree of amplitude accuracy.

C. Memory Matrix Shift Register

In the introduction it was mentioned that each sample on the tape corresponds to a particular instant of time. A simple means for keeping these samples in order is to move the groups of digits, as they are played back, through a multi-channel shift register, as shown in Figure V.

The register shown in Figure V can move groups of three digits from stage to stage by means of advance pulses applied simultaneously to all the memory units. When an advance pulse is applied to a memory unit, it causes the digit in the unit to be moved into some sort of delay element, which feeds the digit into the next memory unit after the advance pulse has ended. This delay prevents interference between incoming digits and the advance pulses.

The variable delay function can now be realized. As the information in the form of groups of digits or "words" moves from stage to stage in the shift register, a counter can keep track of the position of the most advanced word. It can also read it out of the register and into the read-out pulse generator of Figure IV when so ordered by the synchro-

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*Appendix A gives the elementary mathematics of binary digits.

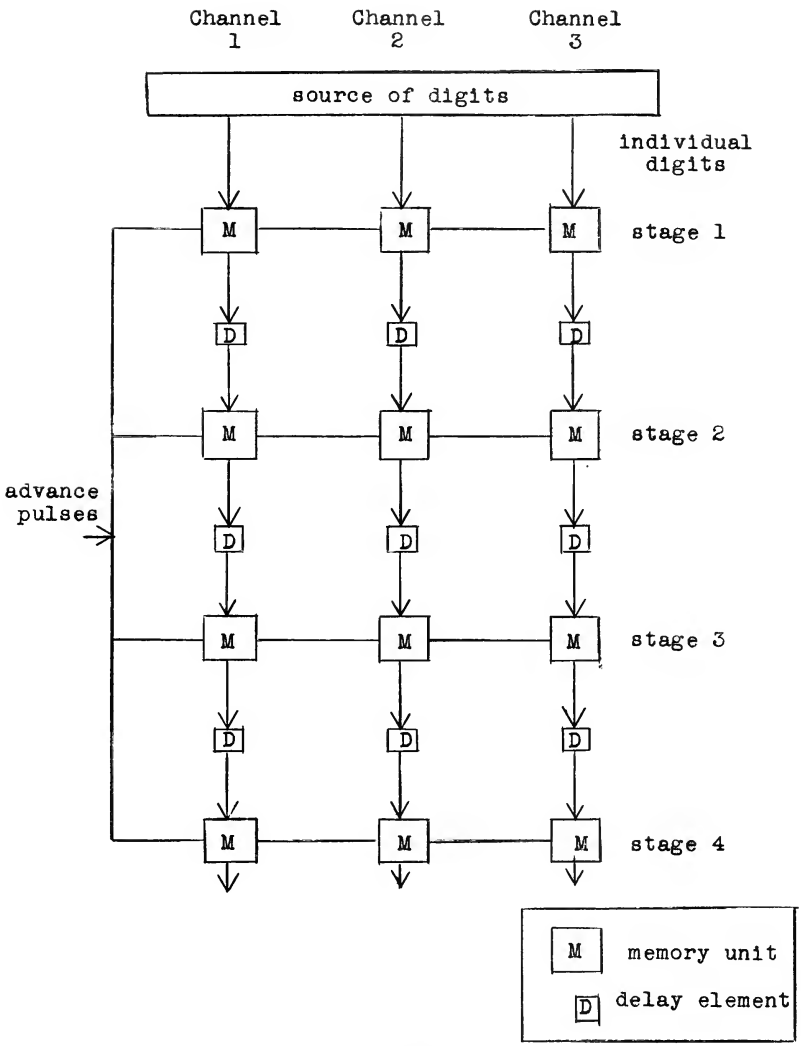


Figure V

Multi-Channel Shift Register

nizing clock pulse.

D. System Limitations

The use of magnetic memories, especially in a shift register, has again implied limitations on the associated apparatus. All of these limitations stem from the fact that a magnetic memory unit can only respond to one stimulus at a time. The limitations are:

1. There must be a delay in the flow of information from unit to unit, as already described.
2. The duration of the advance pulse must be sufficient to switch the cores in the memory units, but shorter than the delay time between units.
3. All inputs must be accomplished in the first stage before the advance pulse is applied.
4. There must be some means of preventing time coincidence between the advance pulse and the clock, or read-out pulse.
5. The system must always be ready to receive and store more information when it is reproduced from the tape. This results from the use of magnetic tape which is continuously in motion and does not stop and wait to be sensed.

Limitations 1 and 2 state a shift time (or shift rate) for the shift register, and for the individual memory units.

Limitation 3 merely states that a "late" digit will not enter the memory unit at the proper time.

Limitation 4 leads to a fundamental pulse rate limitation

on the overall system, and will be discussed in detail shortly.

Limitation 5 implies the existence of a buffer memory stage which is immune to the clock read-out, since the input digits, which are continuously coming off the tape, must have some place to go, if they should occur during a clock pulse.

These limitations can be met in the sub-system shown in Figure VI, which is a block diagram of the Variable Delay Memory Circuit.

E. General Operation of the System

The pulses from the playback transducer are amplified and applied to a synchronizing memory input stage. These input pulses include binary digits and a group marker, with varying amounts of time distortion. The marker samples the digits, then afterwards initiates a new marker or advance pulse, thus meeting limitation 3. (Here it is assumed that the lack of synchronism between pulses is small.) As the digits are sampled, they are stored in magnetic memories; thus limitation 3 is met.

The new marker and a synchronizing clock pulse are applied to an anti-coincidence circuit, which has the function of preventing interference between the two pulses in later operations. This will meet limitation 4 and is described in detail below. The output of the anti-coincidence circuit is non-interfering pulses.

The non-coincident marker is applied to the buffer memory units in the input stage and to a modified multiple shift register called the memory matrix. It is applied to

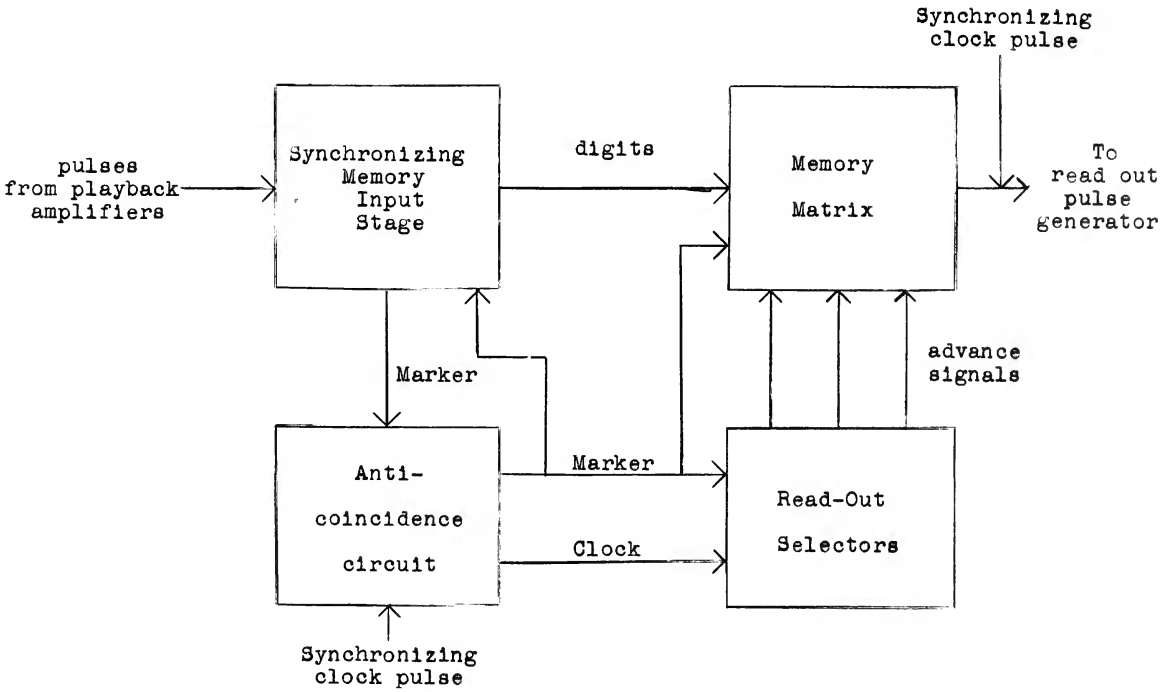


Figure VI

Variable Delay Memory Unit

all advance windings in both places. Thus, with respect to the marker, the system is a multi-channel shift register, and the information still has time distortion as it advances from stage to stage.

The marker and clock are both applied to a combination of memory units and gates in the read-out selectors.

This system selects the group of digits whose turn it is to be read out of the memory matrix and gates the clock into that stage of the memory matrix whenever a clock pulse appears. Since the clock is regular, the output is regular and time distortion has been removed from the information.

Logic diagrams of the four blocks of the variable delay memory unit will now be presented. Circuit diagrams and design techniques are included in Appendix C.

F. Operation of the Synchronizing Memory Input Stage

Figure VII shows the synchronizing memory input stage. It is assumed that the marker and digits do not occur exactly simultaneously, but contain varying small random delays.

The marker input is delayed slightly and then triggers a gate generator. The delay allows any late digits to arrive, but is not long enough for any early digits to have terminated.

Each digit enters via a delay stage, which delays the digit only if it is necessary in order to account for some fixed misalignment of the playback transducers.

The digits and the marker gate pulse are applied to a coincidence marker mixer. This mixer samples the digits

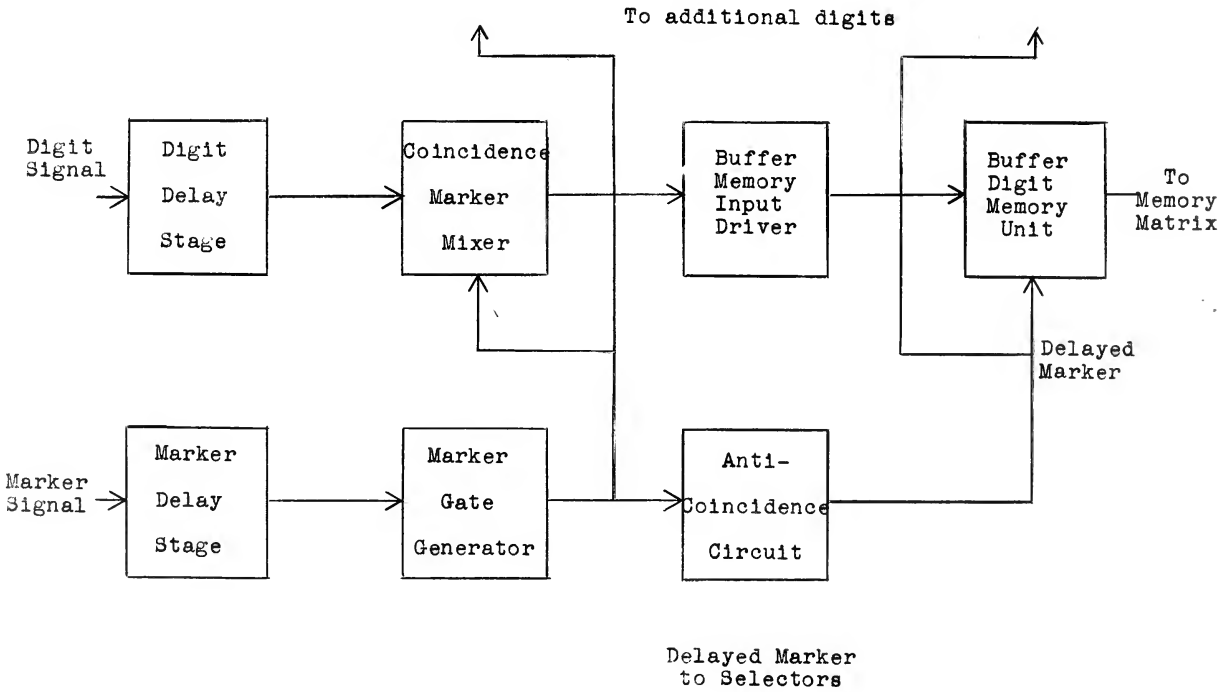


Figure VII

Block Diagram of Synchronizing Memory Input Stage

during the marker gate pulse, thus synchronizing them. The synchronized digits are then stored in the buffer memory units by an input driver.

The end of the marker gate pulse is applied to the anti-coincidence circuit which returns an advance pulse to advance the digits to the memory matrix.

G. Anti-Coincidence Circuit

It has been mentioned that some means of preventing interference between advance, or marker pulses and clock pulses is required. This is Limitation 4, above. The statement was made that Limitation 4 leads to a fundamental limitation on pulse repetition rate for the overall system. Although the basic limitation is obvious, its corollary is not.

The limitation can be stated in another way: since the clock pulses must be perfectly regular, any marker pulse which would interfere must be postponed until such time as it will not interfere.

The logic of the anti-coincidence system devised is shown in Figure VIII. The time analysis corresponding to the method is shown in Figure IX. The following discussion applies to both figures.

In analyzing the function of the anti-coincidence circuit, its final complexity was necessitated by the following considerations.

1) Rise and fall times do not occur instantaneously.

2) There must be sufficient time allowed for the

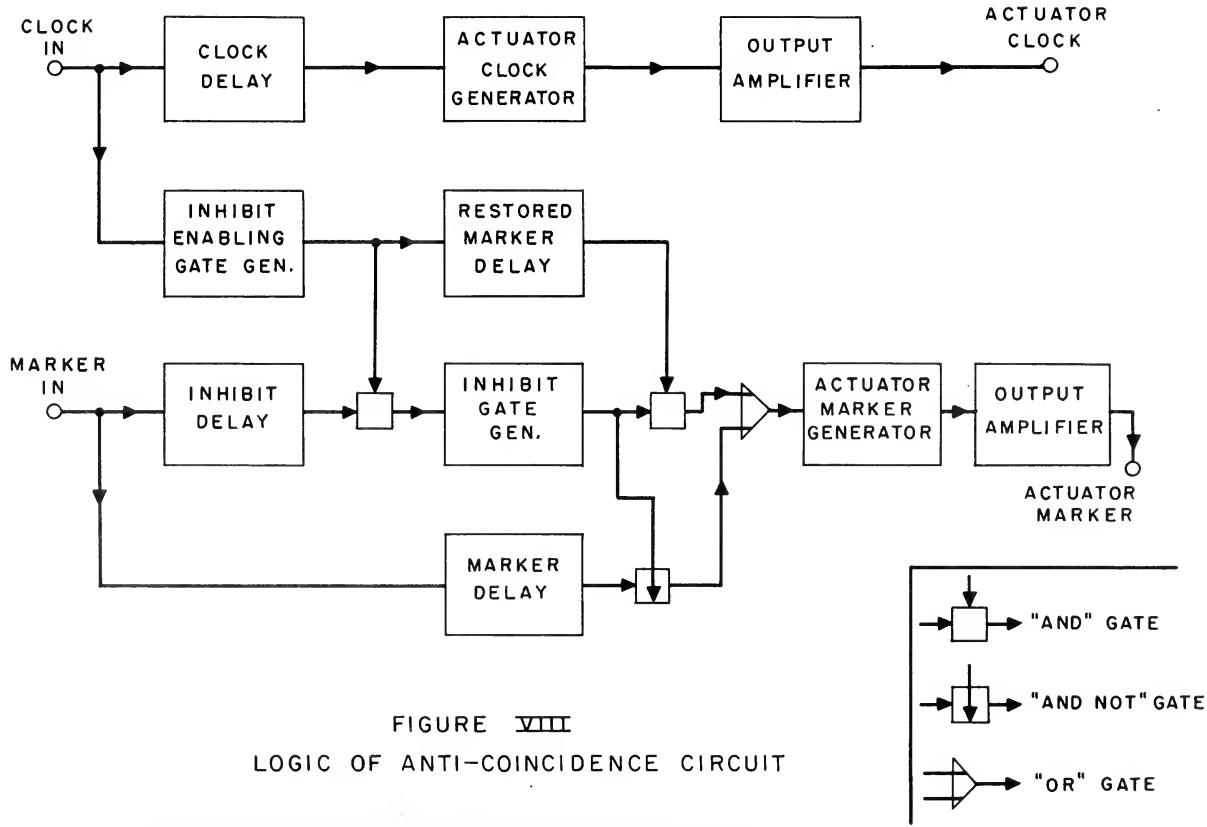


FIGURE VIII

LOGIC OF ANTI-COINCIDENCE CIRCUIT

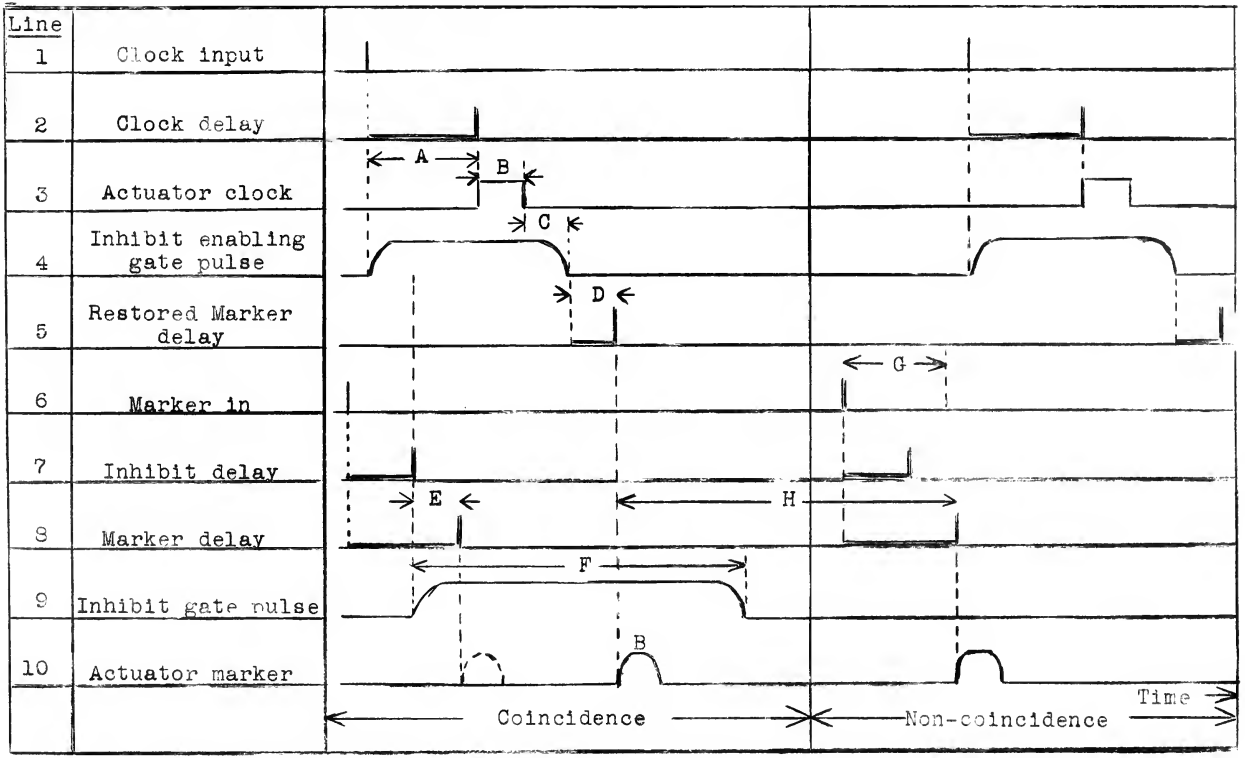


Figure IX

Anti-Coincidence Time Analysis

transients in the circuit to die out.

The following paragraphs present in detail the logic involved in achieving the desired anti-coincidence function.

If a marker pulse advances the information in the memory matrix, there will be a short period of time when the system would not be sensitive to a clock pulse, due to the delay between memory stages. The postpone function must therefore be able to commence before the clock pulse.

A simple method of achieving the implied prediction is to activate the postpone function with a clock pulse, and to initiate a new clock pulse after a short delay. This is shown in the top line of Figure VIII and in lines 1, 2, and 3 of Figure IX. The postpone function is partially accomplished by the inhibit enabling gate, which is initiated by the input clock as shown in the second line of Figure VIII and line 4 of Figure IX. It is only accomplished, though, when it is needed, as has been previously noted.

The marker input pulses are delayed in two separate channels. The inhibit delay, which may be zero, depends on the details of the synchronizing memory input stage. The marker delay must be slightly longer, for a reason to be shown later. The inhibit delay is in line three of Figure VIII and 7 of Figure IX. The marker delay is shown in lines 4 and 8, respectively.

The "and" gate following the inhibit delay block of Figure VIII will give an output only if both of the indicated inputs are present. Assuming the situation shown to the left

of Figure IX, there is coincidence and the two inputs are present. The "and" gate therefore initiates the action of the inhibit gate generator.

The inhibit gate, shown in line 7 of Figure IX, lasts beyond the end of the inhibit enabling gate.

Since coincidence has been assumed, the end of the marker delay occurs during the time of the inhibit gate. Therefore, the "and not" gate shown following the marker delay in Figure VIII does not give an output. If there were no coincidence, there would be no inhibit gate pulse and the marker delay would initiate the actuator marker, as shown in Figure IX, line 10, on the right hand side.

The reason why the marker delay is longer than the inhibit delay is now apparent. There is necessarily a switching transient at the onset of the inhibit gate pulse, and this transient must be allowed to die out before the inhibiting takes place.

For a similar reason, a restored marker delay is necessary if the inhibited marker is to be restored as soon as possible. This delay is initiated by the end of the inhibit enabling gate, as shown in line 5, Figure IX. The "and" gate following the inhibit gate generator will initiate the actuator marker if the end of the restored marker delay occurs during the inhibit gate pulse.

H. Time Analysis

On Figure IX are marked the time intervals of interest. Interval A minus interval E is the total time,

including advance pulse and delay, required to advance digits from memory unit to memory unit. (Limitation 1).

Interval B is the drive pulse duration for the memory units.

Interval C + interval D is the recovery time for the selector arrangement. It is not necessary to allow digits read out by the clock to remain in the memory unit. These digits, once read out, may be forgotten.

Interval D is the fall or decay time of the inhibit gate.

Interval E is the rise time of the inhibit gate.

Interval F must be longer than A + B + C + D, in case the inhibit gate pulse is initiated immediately after the clock input.

Interval G is the difference between the average marker interval (which equals the clock period) and the minimum marker interval. It should be noted that G is not the total time error, but the maximum incremental time error of the marker pulses.

Interval H is the minimum time between a postponed coincident marker pulse and a marker pulse which does not suffer postponement.

From these definitions, the following equation is self-evident:

$$P = \text{Maximum Marker Postponement} = A+B+C+D-E \qquad (1)$$

This postponement represents a time distortion of sorts which has been introduced deliberately in order to avoid interference between actuator marker and actuator clock. An additional time distortion is represented by interval G. Therefore, we can define a maximum equivalent incremental time distortion T.

$$T_{max} = A+B+C+D-E+G \tag{2}$$

The remaining time between actuator marker pulses is interval H, which has a minimum value when the equivalent time distortion is a maximum.

$$H_{min} = \frac{1}{f_c} - T_{max} \tag{3}$$

Where f_c is the clock frequency.

Obviously, H_{min} must be long enough for a complete information shift in the memory matrix.

$$H_{min} = B + M \tag{4}$$

Where M is the necessary memory delay.

Combining (2), (3), and (4),

$$\frac{1}{f_c} = A + 2B + C + D - E + G + M \tag{5}$$

This equation can now be simplified.

$$A = B + M + E \tag{6}$$

$$\frac{1}{f_c} = 3B + 2M + C + D + G \tag{7}$$

By proper attention to design details, we can make the selectors recover as rapidly as we please. Ideally, we can make the selector recovery time C + D reduce to zero.

Furthermore, if the time distortion is of low frequency, then the incremental time error G may become very small for high sampling rates. Thus we can say that, ideally

$$f_c = \frac{1}{3B + 2M} \tag{8}$$

This shows that the clock frequency, and therefore the sampling rate, is less than half the advance rate of the basic shift register.

The marker delay and inhibit delay do not enter into either of the last two equations. The reason is that these delays need not be long ones. It is only essential that they should not be long enough to cause a postponed marker to occur during or after the time when the next marker is reading-in to the synchronizing memory input stage. If this is the case then they have not violated Limitation 5.

The reason for having the inhibit delay at all depends on the source of the marker input. This source may correspond in time to the playback marker from the playback transducer itself, or it may correspond to the beginning or end of the digit read-in gates. It is in any case necessary to allow the read-in function to be completed.

I. Read-Out Selector Logic

The system as described so far has stored the incoming digits in a memory unit matrix and is providing non-coincident clock and marker pulses for read-out and advance of the digits.

It is necessary to keep track of the position of the

most advanced word in the memory matrix and to read out that word with each clock pulse. A method for selecting the most advanced word is shown in logical form in Figure X. A system of memories and gates does the selecting.

The selector memory units shown are continuously sensed by the gates. They are therefore different from the digit memory units, which are sensed only intermittently. The selector memory units have two stable states. A "+" state is caused by receiving an input from the left hand (marker) gate and a "-" state is caused by receiving an input from the right hand (clock) gate.

The operation is as follows: Consider an initial condition of no information stored and all selector memory units in the "-" condition. Then no selector gate is sensitive. If a group of digits is now read into the memory input stage, the accompanying marker will (1) set selector memory unit 1 to the "+" condition, and (2) advance the digits into the memory matrix. After a brief delay, marker gate A and clock gate 1 become sensitive.

There are now two gates which are sensitive. If the next event is a clock pulse it accomplishes the following:

(1) Selector memory unit 1 is switched to the "-" condition.

(2) The clock is applied to stage 1 of the memory matrix.

(3) The "and" gates at the digit outputs are sensitized.

(4) The digits in memory matrix stage 1 are shifted to

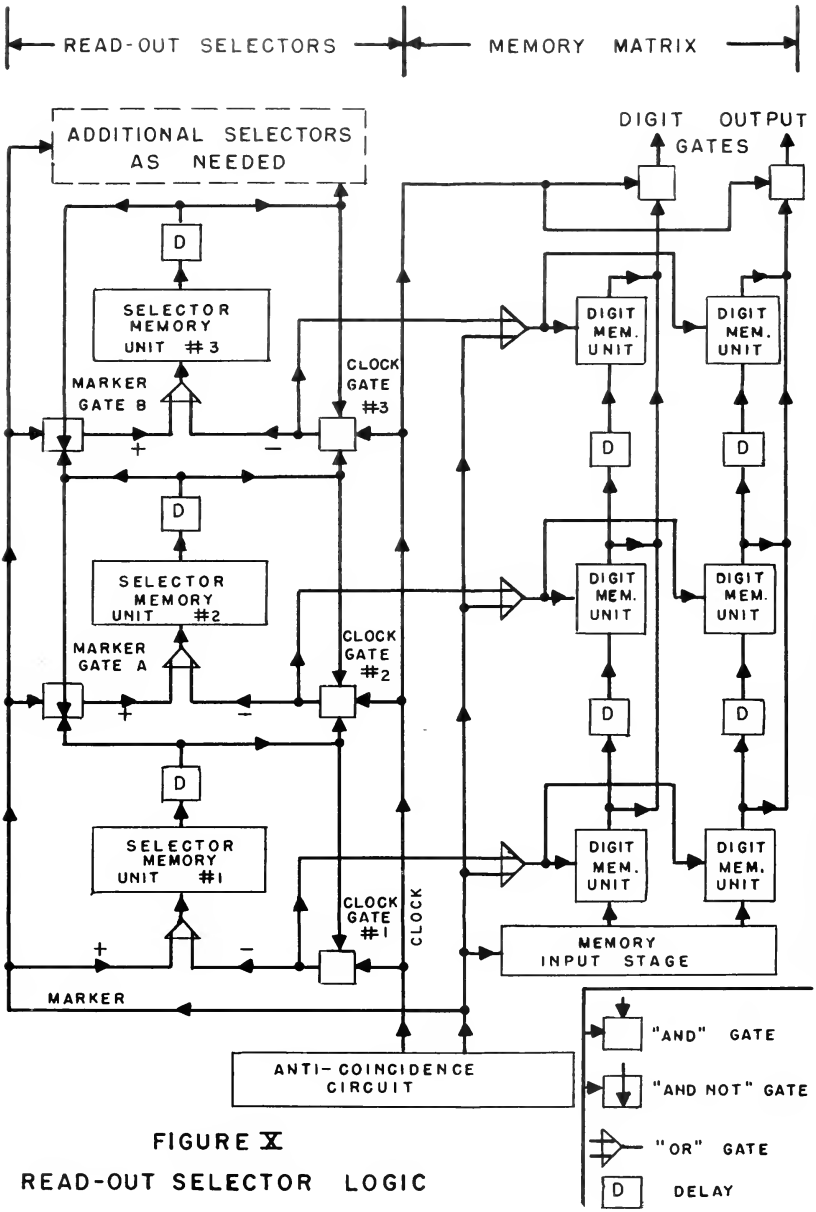


FIGURE X

READ-OUT SELECTOR LOGIC

stage 2, where they are out of reach and "forgotten."

(5) As the digits come out of the stage 1 memory units, they are also sensed by the digit output "and" gates. Since these gates are sensitized during this time, the digits are read out through the gates.

(6) After a short delay, clock gate 1 and marker gate A are desensitized.

If the event had not been a clock pulse, but had been a marker pulse, then it would have accomplished the following:

(1) Selector memory unit 2 would be switched to the "+" condition.

(2) The digits in memory matrix stage 1 would be advanced to stage 2. New digits would be stored in stage 1.

(3) After a short delay, clock gate 2 and marker gate B would be sensitive.

Continued analysis shows that the selectors are merely unit counters which can add or subtract one digit at a time. The gates corresponding to the change from "+" to "-" in the selectors indicate where digits can be inserted. Marker inputs add one "+" and independently shift all digits in the matrix. Clock inputs subtract one "+" and read out the single stage of digits corresponding to the "+" subtracted.

The digit output "and" gates will have concurrent

inputs only when there is a clock pulse applied to the system. Marker pulses may cause some small transmission, depending on the details of the gating circuit, but cannot cause full output, since there is no clock pulse applied simultaneously.

The delay between selectors must be long enough to prevent a chain reaction to a single clock or marker pulse. If excessive, it contributes to the effective selector recovery time and limits the playback rate, and therefore the initial sampling rate.

Terminal gating arrangements on the selectors can be simpler, as shown for selector memory unit 1. In this case, there is no marker gate at all, for any marker pulse corresponds to information being stored in the first memory matrix stage.

Although the marker gate has been omitted entirely from the initial stage, the clock gate may not be omitted entirely from the final stage. The clock must only be able to sense the final digit memory stage when it is desired; otherwise it is possible for it to read-out "forgotten" information.

J. Circuit Details

The circuits which are required to accomplish the functions so far described were designed, constructed, and tested. Details of techniques and schematic diagrams are set forth in the Appendix.

K. Desired Result

The proof of the operation of the system described would be a single stationary oscilloscope pattern showing a pre-

viously recorded repetitive sequence of digits being played back without time distortion. A similar, but moving, pattern showing the same sequence of digits with time distortion might appear as a low-amplitude background or noise. Figure XI shows a possible digit sequence and the anticipated resulting pattern.

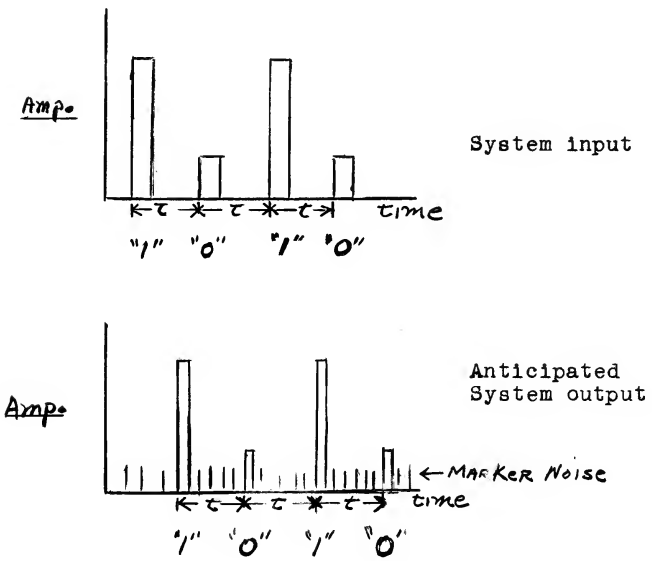


Figure XI

Oscilloscope pattern
for desired result

L. Evaluation of Tape Recorder

The special machinery actually on hand at the beginning of this thesis consisted of an Ampex Model 307 seven channel tape recorder, including the tape transport or "top plate" and seven electronic chassis. Each chassis included a

complete record amplifier with bias oscillator and a complete playback amplifier. An instruction manual was available which included over-all specifications on the machine and schematic diagrams of the components.

The instruction manual gave the following characteristics for the recorder operating at a tape speed of 60 inches per second:

TABLE II

Ampex Model 307 Tape Recorder Specifications [3]

Frequency response: ± 3 db 200 to 80,000 cps down no more than 10 db at 100 and 100,000 cps

Tape saturation 20 db above recommended operating level. Tape used was 1 mil oxide on 1 mil mylar.

Flutter and wow: Well under 0.1% rms, measuring all flutter components from 0 to 300 cps using a tone of 3,000 cps.

Record amplifier normal operating input 1.23 volts rms.

Playback amplifier - normal output 1.23 volts rms.

Harmonic distortion: Less than 1% rms.

It was recognized at the outset that the recorder was not intended for pulse work. The rather complete specifications given above and in the manual are quite uninformative when the recorder is to be used for pulse recording. For example, wow is given as a percentage. The information needed is the maximum total time (or position) error in the record-playback process, since this error governs the number of stages required in the selectors and memory matrix.

Frequency response of the recorder as a system is given

in terms of an upper limit. Step-input transient response is more desired, because of the intrinsically transient nature of pulses. More information about the record and playback heads is needed. Recorder characteristics for this thesis were obtained both experimentally and analytically.

M. Pulse Response of an Ideal Tape System - Analytic

In order to determine the pulse response of an ideal tape system, an investigation of a tape moving with velocity v over the record and playback heads, each having an air gap of width d, is considered. A square pulse of magnetization of duration t is assumed applied to the record head. All self-inductance effects, fringing effects, and effects of tape thickness and material are neglected. The system thus described will now be treated as an ideal system.

The magnetized spot on the tape will be of length ℓ.

$$\ell = d + vt \tag{9}$$

On playback, the spot will influence the playback head from the instant the leading edge of the spot enters the air gap until the instant the trailing edge leaves the gap, for a total distance of $d + \ell$. Therefore the pulse is stretched to a new duration t_1.

$$t_1 = \frac{d+\ell}{v} = \frac{2d}{v} + t \tag{10}$$

Ideally, t = 0, but practically, t must be long enough to overcome the self-inductance of the record head.

The playback waveform will not be an ideal square pulse. The influence of the ideal magnetized spot on the tape starts at zero with the leading edge of the spot entering the gap,

rises uniformly to a maximum value as the leading edge crosses the gap, remains at the maximum until the trailing edge enters the gap, and then falls uniformly to zero as the trailing edge crosses the gap. The differentiation caused by the head itself will then cause the output voltage to be two ideal square pulses of opposite polarity, each with a duration $\frac{d}{v}$ and with a dead space in between of t.

These waveforms are shown in Figure XII.

The net effect of ideal tape recording and playback on pulses is then seen to be a direct reproduction, followed by a delay, followed by an inverted reproduction. The pulses reproduced do not depend on the recorded pulse length, but the delay does.

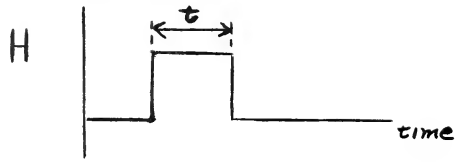
In a practical system, the output pulses will be rounded and, perhaps, stretched due to the fringing effects and transducer time constants. The input pulse must therefore be long enough to prevent excessive interference between the two output pulses it causes.

N. Determination of Transducer Characteristics

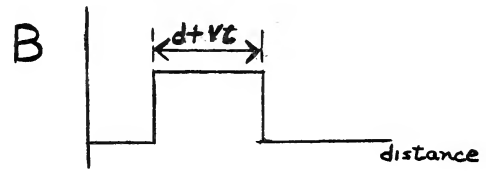
The method for determining the pulse characteristics of the Ampex heads and tape consisted of recording pulses of varying strength and duration and playing them back through a wide-band (video) amplifier.

The recording equipment consisted of a one-shot multivibrator driving a pentode current amplifier. A pentode was chosen because of the constant-current characteristic obtainable, and the ease of current variation by changing screen

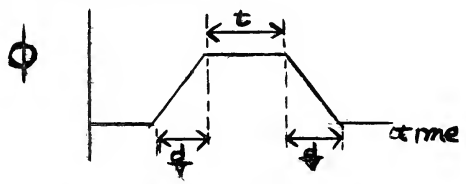
a) Input to ideal record head



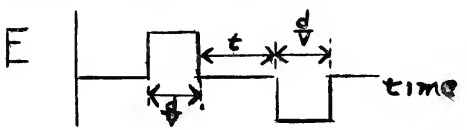
b) Spot recorded on tape, ideal



c) Ideal playback gap flux



d) Ideal playback head output



e) Probable playback waveform from actual head

Figure XII

Ideal Pulse Recording

grid potential. The pulse length was varied by varying time constants in the multivibrator. A bias current was applied to the record head so that the steady state would correspond to one polarity of magnetization, and the recorded pulses would correspond to the opposite polarity.

The video amplifier consisted of two pentode amplifier stages followed by an over-biased triode. The object here was to make the triode respond only to the first pulse of the two played back.

Schematic diagrams for the special record driver and video amplifiers are given in the Appendix.

O. Measurement of Time Distortion

Time distortion was measured on an oscilloscope by means of a Lissajou figure and also with a method involving a linear sweep.

The Lissajou figure method is described as follows: If a recorded sine wave is displayed on the oscilloscope X axis, and a sine wave from a stable source of the same frequency is displayed on the Y axis, the net effect will be an elliptical pattern. If there is no time distortion in the played back sine wave, then the pattern will be stationary. If the phase relationship between the two waves is just right, the ellipse may degenerate into a straight line.

Time distortion is equivalent to phase modulation of the playback sine wave. A time error of e seconds will correspond to a phase change of 360 ef degrees, where f is the average frequency.

The straight line pattern is obtained for four different phase relationships 90^{o} apart. If the Lissajou pattern varies between two of them, then the maximum peak-to-peak phase error is 90^{o}. Such a varying pattern is ambiguous because it may represent "passing through," rather than "stopping." On the other hand, if the Lissajou pattern almost closes, then there is no ambiguity.

By changing the frequency of the signal source, we can find a frequency such that the maximum peak-to-peak phase error is slightly less than 90^{o}, and the oscilloscope pattern can be made to vary between two very narrow ellipses. In such a case we can say

$$e = \frac{1}{4f} \tag{11}$$

In the linear sweep method, pulses of short duration and low frequency are recorded and played back. The playback pulses are displayed on a linear sweep with the oscilloscope synchronized from an external source of the same frequency as the original pulse repetition frequency.

If there is no time distortion, then there will be a steady pattern presented. If there is time distortion, the pulse displayed on the oscilloscope screen will swing back and forth. The total excursion of a point on the pattern represents the maximum peak-to-peak time distortion directly, and is unambiguous. Long-term effects will show up as a slow drift of the swinging pattern.

P. Test Programming

The individual chassis were tested and adjusted when

they were constructed. The entire system was tested as a group when all the chassis were completed.

Proper testing required test program generators. A special program generator was built for testing the anti-coincidence circuit and the read-out selectors; square wave generators sufficed for programming the over-all system.

The program generator built for testing the anti-coincidence circuit consisted of two one-shot multivibrators triggered simultaneously from an external square wave generator. One of the multivibrators had a fixed period of 50 microseconds. The other had a period variable from 35 to 65 microseconds. The fixed-period multivibrator was used to provide a simulated clock input to the anti-coincidence circuit. The variable-period multivibrator provided a simulated marker input which could be "passed through" the clock input. Thus it was possible to simulate coincidence and near-coincidence, and to observe the operation of the anti-coincidence circuit through the full range of its operation.

The testing of the selectors required the same program generator and the anti-coincidence circuit. It can be seen that passing the marker through the clock is equivalent to adding or subtracting one and only one marker pulse, depending on the direction. Thus, given an initial condition in the selector memory units, each selector can be tested for its own operation and operation of the associated clock and marker gates.

For programming digit inputs to the record pulse generators

and head drivers, square wave generators were used. One was triggered at a frequency of 5000 cps by a 10,000 cps secondary frequency standard, and provided a trigger for marker recording. It also triggered two other square wave generators, one operating at 5000 cps and one operating at 2500 cps. These in turn provided triggers for digit channels, with two different programs. The 5000 cps trigger was of the same frequency as the marker and therefore corresponded to a program of ones. The 2500 cps trigger was half the marker frequency and therefore corresponded to a program of alternate ones and zeros.

The program of ones did not lend itself well to testing, since all ones are alike. The program of alternate ones and zeros was quite satisfactory because the successive digits can be distinguished from each other. This is the program shown in Figure XI as a hypothetical input. The same program as played back is shown in the Results section in Figure XV.

Q. Resume of Procedure

The procedure of this thesis followed two concurrent paths. One was the development of the general system, the other was the evaluation of the recorder available.

The development of the general system consisted of the following steps:

1. The decision to use magnetic memory units.
2. An analysis of the special techniques thus required, e.g. anti-coincidence and synchronizing inputs.
3. Time analysis. Equation 8 was derived and shows that the maximum sampling frequency is slightly less than

half the maximum shift frequency of the magnetic shift register used in the memory matrix.

4. Selector logic development.
5. Design and construction of the circuitry required. Details of this portion are to be found in the appendix.

The evaluation of the recorder consisted of the following steps:

1. Analytical investigation of pulse recording and playback.
2. Experimental investigation of the pulse characteristics of the record and playback transducers and tape, considered as a network. Pulse duration and record head drive current were considered.
3. Comparison of the experimental record head drivers and playback amplifiers with the regular Ampex equipment that was available.
4. Measurement of time distortion (wow).

The procedure was terminated by evaluating the performance of the individual units constructed for the system and of the units combined into a complete system. This required a simple program generator.

III. RESULTS

A. Extent of Results

The results from evaluating the Ampex recorder used and the experimental equipment developed may be placed in the following categories.

Transducer characteristics

Amplifier characteristics

Time distortion

Head alignment

Operation of complete system

The above divisions indicate the major problems that were encountered in the pulse recording and operation of the Variable Delay Memory Unit.

B. Transducer Characteristics

The amplified playback waveform from the magnetic tape is shown in Figure XIIIa. The following conditions for recording and playback amplification existed:

Recording

Bias current in record head	−7 ma
Drive current in record head	28 ma
Drive current pulse length	12 μsec.
Drive current rise and fall time	$\frac{1}{2}$ μsec.

Playback

Playback amplifier	2 stage video amplifier using 6AK5 tubes (Appendix No.)
Peak output voltage of playback head	-20 millivolts
Output voltage at V605 (Figure XIIIa)	28 volts

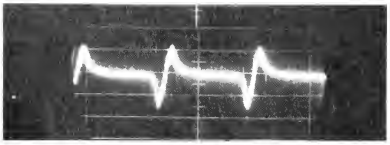


Figure XIII(a)
Playback pulse waveform (50 μs/cm)
Input pulse was 12 us, square

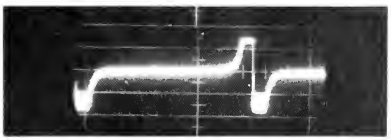


Figure XIII(b)
Effects of overdriving Ampex amplifier
50 μs/cm

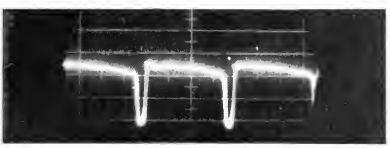


Figure XIII(c)
Effects of overdriving
experimental amplifier
50 μs/cm

Under normal conditions the same record pulse played back through the Ampex amplifier produced the same waveform as Figure XIIIa.

The drive current for recording the pulses was determined as follows: The Ampex specifications and Ampex circuit components indicate that a normal level of input (1.23 volts rms) corresponds to about a 7 ma rms record current at the record head. The bias currents were varied from zero to 18 ma but showed no effect in the recording capabilities of the head. Peak drive currents from 20 ma to 47 ma had no effect on playback waveform or duration. No saturation effects were observed with peak drive currents of 47 ma. The drive current pulse length produced the following effects:

Pulse durations shorter than 10 μsec. produced no playback output.

Pulse durations from 10 to 20 μsec. produced essentially the same output waveform as shown in Figure XIIIa.

Shortest playback pulse was obtained from a drive pulse of 12 μsec.

The above measurements were made on tape channel 3.

An unexpected problem which developed during the use of the recorder was "wander" during the recording and playback processes. The tape drifted laterally causing very poor pulses to be played back. When it occurred the playback pulses on all channels were intermittent and the system operation was quite spasmodic.

C. Amplifier Characteristics

Figure XIIIb shows the effects of overdriving Ampex amplifiers (by adjustment of playback level control, Ampex component R2714). Peak-to-peak amplitude -40 volts.

Figure XIIIc shows the effects of overdriving the experimental playback amplifier. Output was taken from the plate of V606.

D. Time Distortion

Figure XIV gives oscilloscope pictures of a playback pulse, self-synchronized; a 10 KC timing wave; and a playback pulse, externally synchronized. The photograph was made with simultaneous record and playback at a 1 second exposure.

The wow picture of Figure XIV is not a true representation of wow. With record and playback on separate runs, the time distortion was estimated to be 200 μsec. peak-to-peak. The presentation had a slow drift, even though the capstan motor was driven from a 60 cps frequency standard. Because of this, no photograph could be obtained to give a true representation of the time distortion present.

The primary wow frequency was variable, but averaged about 3 cps. The slow drift had a frequency of about $\frac{1}{4}$ to $\frac{1}{2}$ cps, and was very large, perhaps several milliseconds. The tape seemed to slip slightly occasionally; therefore, this figure could only be estimated.

When wow was measured with a Lissajou figure, the ellipse did not quite close at a recording frequency of 7000 cps. Again, it was impossible to get a reliable measurement

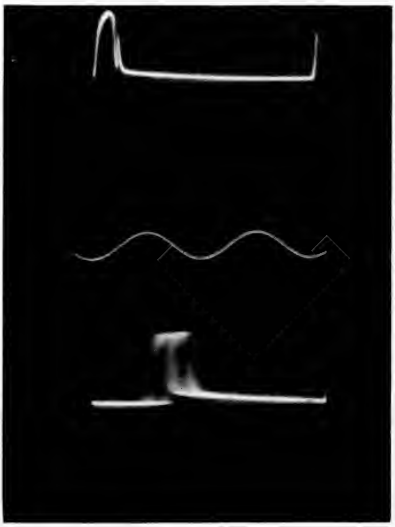


Figure XIV
Time distortion - linear sweep
50 μs/cm

Top - playback pulse, self-sync.

Center - 10 kc timing wave

Bottom - playback pulse, clock sync.

unless record and playback were simultaneous.

E. Head Alignment

There appeared to be slight relative misalignments in the heads, such that pulses recorded simultaneously on several heads did not play back simultaneously, but had errors of several microseconds. With respect to channel 3, channel 4 was 20 microseconds early and channel 5 was 40 microseconds early.

F. Operation of Complete System

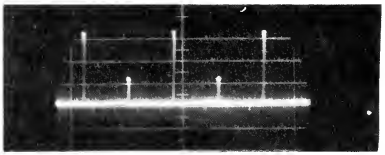
1. The anti-coincidence circuit operated properly at clock frequencies up to 20,000 cps.

2. Five of the six selectors constructed operated properly. The sixth would not switch.

3. The synchronizing memory input stage operated properly. Figure XV shows an alternate one-zero pattern at the grid of the memory unit read-in driver, V103A.

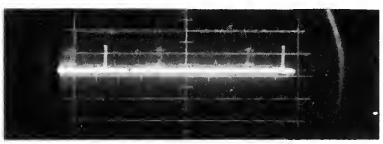
4. The memory matrix operated properly as a shift register. The digit output gates operated properly when the digit groups were read out by a clock pulse. The background noise level due to marker pulses advancing the digits, was high, about 1/3 of the clock pulse amplitude.

5. The overall system, because of the one bad selector, did not operate properly. The oscilloscope presentation desired, as shown in Figure XV, was obtained, but when the marker "passed through" the clock, the "ones" and "zeros" interchanged, indicating failure of the selectors to perform their function.



1 0 1 0 1

Figure XV
Input program
Alternate ones and zeros
at grid of V103A
100μs/cm
14 v/cm



1 0 1

Figure XVI
Output waveform
Alternate ones and zeros
at output of memory matrix
200 μs/cm
14 v/cm

6. A photograph (Figure XVI) was obtained between jumps of the oscilloscope pattern. This photograph shows the desired pattern, and conceals the discrepancy known to exist in the system.

7. Although the tape capstan motor was driven from a 60 cps frequency standard, and the recorded pulses were timed from a 10 kc frequency standard, the playback clock had to be slightly off 10 kc in order to stop the oscilloscope pattern at all. A precision variable frequency oscillator (Navy type LP-5) was used.

IV. DISCUSSION OF RESULTS

A. Feasibility of Method

Although the one bad selector prevented the system from operating satisfactorily, the results obtained from tests of the individual selectors, and the fact that the proper response of the system was obtained for short periods, indicate that the proposed method is quite feasible.

The limitations on the method are (1) the limitations imposed by the use of magnetic memories, already discussed in the Procedure, and (2) the limitations imposed by the basic recording system.

The first limitation can be dismissed temporarily by putting numbers into equation (7).

$$\frac{1}{f_c} = 3B + 2M + C + D + G \qquad (7)$$

For the memory units used B = 1 μs, M = 2½ μsec.

For the selectors built, C + D = 4 μsec.

For the recorder used and any sampling rate above 10,000 cps, G = 0.

Therefore $\frac{1}{f_c} = 12\,\mu\text{sec}.$

$$f_c = 83{,}000 \text{ cps}. \qquad (12)$$

This figure gives such a high allowable sampling frequency that the true limitation on the method is in the basic recording and playback apparatus, which cannot at present be operated at such pulse rates. Furthermore, a more elegant design of the selectors, and the use of available higher-speed memory units, could easily push the

sampling frequency, f_c, up by a factor of two.

On the other hand, the basic recording system imposes severe restrictions. It can be seen from equation (10) that, with a typical head gap of 0.001 in., and a typical tape speed of 60 ips, the playback pulse will last at least 33 μsec. Add to that the drive pulse length and some small fringing effects and the playback pulse lasts for 50 μsec. This is the result actually obtained, as shown in Figure XIIIa. Since most of the playback pulse length is caused by gap distance and tape velocity, there is little that can be gained by improving tape materials or electronic components. Attention must instead be focussed on making $\frac{d}{v}$ small.

The 50 μsec playback pulse means that the basic recorder is limited to pulse rates of about 20,000 pulses per second. Pulses were actually recorded at this frequency although at this point the playback pulses had already begun to interfere with each other. This corresponded to a stacking density of roughly 300 pulses to the inch.

The recording current amplitude affected only output voltage amplitude, as might be expected. The value of having a bias current is small, although it would tend to erase any noise on the tape. This supports the conclusion drawn above, that improving electronic components will gain little in over-all characteristics.

In time distortion, there is a different situation. The entire purpose of this thesis was to circumvent time distortion by means of electronic apparatus external to the tape transport mechanism. The results obtained indicate a

good degree of success, in spite of the weak link in the selectors.

The basic time distortion present had a peak-to-peak extent of about 200 μsec, and a frequency of about 3 cps. The long term drift may have been due to slippage of the drive capstan, or to some intrinsic property of the tape or tape transport. However, since it was possible to follow the drift by hand, as was done to obtain Figure XVI, the drift is something which can be corrected. The most obvious approach is a positional servomechanism capable of correcting the long term errors, and thus complementing the selectors. Such a servomechanism might even be able to reduce part of the basic time distortion, and thus reduce the number of selector and memory matrix stages required.

The essential method of eliminating time distortion is still the variable delay process, involving the selectors and magnetic memories, since a servo probably could not follow all the time errors involved. An error signal can be picked off from the selector flip-flops themselves to indicate the "fullness" of the matrix, and this error signal can be the input to the positional servo required.

The total capacity of the selector-matrix combination must be at least equivalent to the peak-to-peak time error in the playback pulses. For any given error, the number of stages required is proportional to the sampling frequency, because the capacity of one stage is one sampling interval. Thus, for a 20,000 cps sampling rate and a 200 μsec peak-to-peak time error, only four stages would be required. This

result indicates that the system need not be very extensive.

It should be remembered in evaluating the time distortion results that Figure XIV does not represent all the wow present, because of the artificial means of stabilizing the oscilloscope presentation.

B. Recorder and Playback Characteristics

The slight relative misalignment of the heads on the machine used indicates a need for some means of mechanical or electrical compensation. A position error of only 0.001 inch is equivalent to a time error of 17 μsec at a tape speed of 60 ips. Therefore some electrical compensation, such as a delay line, would probably be necessary.

The unexpected problem of wander indicates a need for a better guide system to keep the tape from buckling against the guides as it slides over the heads.

The comparison between the Ampex playback amplifier and the experimental video amplifier (Figure XIII) does not indicate any significant qualitative superiority of either when used for pulse playback. The experimental amplifier does have the advantage of simplicity and low power consumption, since it is not required to have good low-frequency performance. Accordingly, similar small amplifiers are recommended for use in any future investigations along the line of this thesis. On the other hand the squaring output stage of the experimental amplifier cannot be recommended in spite of the good results obtained (Figure XIIIc), because it is not able to take advantage of the mid-pulse crossover

shown in Figure XIIIa and b. This crossover is the most detectable change in the playback pulse if any unforeseen conditions should reduce its amplitude.

The pulse characteristics of the recorder were obtained using 1 mil oxide on 1 mil mylar tape. It is realized that varying the tape composition and thickness could influence the results obtained, but these effects were not considered in any way in this thesis.

V. CONCLUSIONS

1. The proposed method for eliminating time and amplitude distortion in recording, i.e., sampling and coding, is feasible and practical.
2. Transducer air gaps and tape velocity are the primary limitations on sampling rate in such a system.
3. A positional servomechanism is needed to correct for any accumulated long-term position errors in the tape transport mechanism.
4. The relative alignment of the individual channels of the tape heads must be corrected, either mechanically or electrically, to give exact alignment.
5. The playback amplifiers do not need to be large. Simple two- or three-tube amplifiers are satisfactory.
6. The other components constructed were satisfactory, except for a single stage of the selectors, which prevented the system from operating as intended.
7. Equations were developed for determining the maximum sampling frequency.

The lower limit on sampling interval is given by equation (7).

$$\frac{1}{f_c} = 3B + 2M + C + D + G \qquad (7)$$

In the ideal case, $C + D + G \longrightarrow 0$ and the maximum sampling frequency is

$$f_c = \frac{1}{3B + 2M} \qquad (8)$$

Where B is memory unit drive pulse length, M is memory unit delay time, and C, D, and G are as shown in Figure IX.

The duration of playback pulse effects is given by equation (10).

$$t_l = \frac{2d}{v} + t \qquad (10)$$

Where t_l is playback pulse length, d is gap length, v is tape speed, and t is record pulse length. Waveforms are given in Figures XII and XIII.

VI. RECOMMENDATIONS

1. Smaller transducer gaps or higher tape speeds if possible should be used to reduce $\frac{d}{v}$ if high sampling rates (e.g. 50 KC) are desired.
2. A positional servomechanism should be used to drive the tape capstan.
3. A means for preventing "wander" in the tape alignment should be provided.
4. A means for aligning precisely the individual channels of the transducers in a multi-channel recorder should be provided.
5. Playback amplifiers should be designed to take advantage of the mid-pulse crossover in the playback head waveform.

VII. APPENDIX

APPENDIX A

Supplementary Introduction

1. The Mathematics of Sampling

The following analysis, while not a rigorous proof, is a simple demonstration of the Hartley-Shannon sampling law, [which may be stated thus:

> In order for periodic samples to represent a waveform completely, the sampling frequency must be at least twice the frequency of the highest-frequency component of the sampled waveform. [4]

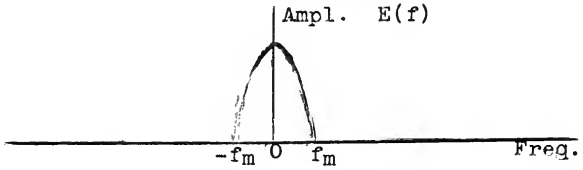
Suppose that a waveform has the amplitude-frequency spectrum shown in Figure XVIIa, and is sampled periodically by an impulse of repetition rate or frequency f_s. This sampling corresponds to multiplication in the time domain or convolution in the frequency domain. The time domain representation of sampling was shown in the text in Figure III.

The convolution process shifts the spectrum of the original wave (Figure XVIIa) to the center frequency of each of the individual components of the spectrum of the sampling wave (Figure XVIIb), giving the result shown in Figure XVIIc.

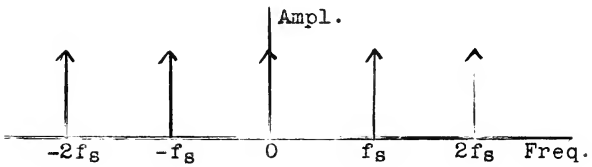
The information in the sampled wave can be recovered from the samples by filtering the samples so that only that portion of the spectrum which represents the original waveform is recovered from the samples. This requires only a low-pass filter.

If the sampling frequency is too low, then the shifted positions of the original spectrum will overlap, and no

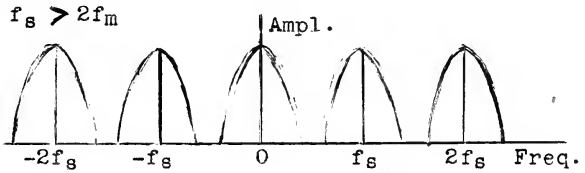
a) Spectrum of original waveform



b) Spectrum of a periodic impulse



c) Spectrum of the original waveform after sampling



d) Spectrum of the original waveform after sampling

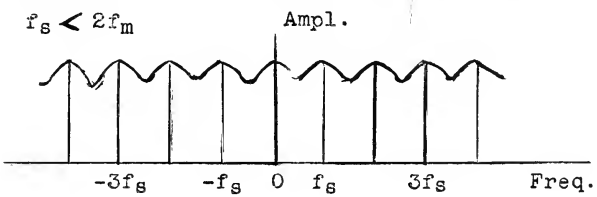


Figure XVII

Spectra Illustrating the Hartley-Shannon Law

portion of the sample spectrum will represent the original spectrum. Such a condition is shown in Figure XVIId. This condition will arise when the sampling frequency is less than twice the highest frequency present in the original waveform.

2. Binary Numbers

The binary system of numbers is a system involving only two digit symbols, which may be "1" and "0", "+" and "-", or "on" and "off". In such a system, our decimal 2 would equal binary 10 and decimal 3 would equal binary 11.

Since a digit in any position can have only two values, a binary number of n digits can represent only 2^n different quantities, the same as a decimal number of n digits can represent 10^n quantities.

As stated in the text of this thesis, the advantage of binary digits is their extreme simplicity. An on-off system can be thought of as a group of randomly selected light bulbs in digit positions. Bright or dim, red or blue, "on" and "off" still mean the same. Any other system would require the lights to be, perhaps, "on-bright", "on-dim", or "off", if the system involves three possible digit values. Amplitude distortion can make strong pulses into weak ones, but if they all have the same significance, there is nothing lost.

APPENDIX B

Circuit Details

1. Synchronizing Memory Input Stage

The general purpose of this component is to transfer pulses from the tape playback amplifiers into magnetic memory units. They are synchronized with the marker channel for reasons described in the text.

The synchronizing part of the circuit is the marker channel, shown schematically in Figure XXb. The input to this channel is taken from the experimental video amplifier, which gives a negative pulse output corresponding to the first portion of the playback pulse of XIIIa.

The negative input pulse cuts off V104A very quickly, causing a sharp rise in the voltage at its plate. This rise triggers the marker delay generator, V105. The delay is needed for two reasons: (1) the digit channels are triggered by the mid-pulse crossover shown in Figure XIIIa, and (2) the marker delay should be extended to sample the middle of the digit pulses.

The marker gate generator, V106, is triggered after the marker delay and provides a negative-going 5 μsec gating pulse for synchronizing and memory unit read-in. V102B is a cathode follower which routes the gating pulse to all the digit channels.

A single digit channel is shown in Figure XXa. This channel is designed to take full advantage of the mid-pulse crossover.

The input network C101 - R101 - D101 causes the changing voltage at the crossover time to trigger digit gate generator V101. The output pulse of V101 is D.C. - coupled to the coincidence marker stage, V102.

V102 can receive inputs on both grids. If it receives only the negative-going marker gate pulse, its voltage output across R113 is an 18-volt positive pulse. If it receives the marker gate during a digit gate pulse, its output is 40 volts. These two conditions are inputs of "zero" and "one", respectively.

The gated digits are applied to the grid of V103A. This tube is biased 40 volts below cutoff. A "zero" input does not raise the level of the grid sufficiently to cause conduction. A "one" input causes full conduction and reads a "one" into the single memory unit connected to the plate of V103A.

The trigger for the anti-coincidence circuit is taken from the plate of V106. Because it comes at the beginning of the marker gate, the marker delay in the anti-coincidence circuit must be at least as long as the marker gate.

2. Anti-coincidence Circuit

The delays and gate pulses in the anti-coincidence circuit are all generated by one-shot multivibrators, as shown in Figure XXI.

A clock input from an external source is applied to V201, which generates the clock delay. At the end of the delay, the rising cathode voltage of V201 triggers actuator clock generator V202. The 1-μsec actuator clock pulse is

inverted by V203, which is D.C. - coupled to clock output connector J202. The output at J202 is normally +180 volts D.C., but drops to +150 volts during a clock pulse.

The clock input is also coupled to V204, which generates an inhibit enabling gate pulse. At the end of this pulse the restored pulse generator is triggered.

The marker input from the synchronizing memory input stage comes in at J203, and triggers both the inhibit delay and the marker delay.

If the end of the inhibit delay occurs during an inhibit enabling gate pulse, then the D.C. level of the input grid of the inhibit gate generator, V207 and V208, is sufficient for the additional pip coupled through C217 to trigger the multivibrator action. The cathode potential of V207 then falls almost to zero, and this cathode potential performs the various gating functions.

"And not" gate V209B will ordinarily conduct at the end of the marker delay pulse generated by V210. However, if the end of that pulse occurs during the inhibit gate pulse, the grid potential of V209B is lowered by current flowing through D202 and R256, and the gating function can therefore be seen to take place in the presence of the delayed trigger from V210 and in the absence of a pulse from V207.

"And" gate V209A will conduct only if its cathode potential is lowered by V207 when the restored marker delay ends.

It can be seen that, for every marker pulse input, either V209B or V209A will conduct, thus triggering actuator marker generator V211. Marker output stage V212 then inverts the pulse in the same way as V203 inverted the clock pulse.

The reason for cathode follower V208 in the middle of the inhibit gate generator is that R241 must be so large for proper gating that the recovery time of the multivibrator would otherwise be too long.

3. Read-Out Selectors and Core Drivers

The selector schematic, Figure XXII shown shows only three of the six stages constructed, the two terminal stages and one of the four identical intermediate stages.

The selector memory units are electronic flip-flops: V302, V306, and V310.

The gating tubes are V301, V302, V309, and V310. The operation of V301B and V301A will be described.

Assume that the initial condition is that digits are stored in memory stage 1. The left hand section of V310, and the right hand sections of V306 and V302 are conducting. Then the grids of V301B, V309A, V311A are at a potential of approximately +150 volts, and the other gate tube grids are at approximately +125 volts. All gate tube cathodes are normally at +180 volts, so they are all cut off.

If now a marker pulse is received at J302 (from J204), the cathode potentials of V301A, V301B, and V309A will all be lowered to +150 volts. V301B conducts, switching V306. V309A also conducts, but does not switch V310 because it is already in the "+" state.

At the same time, the marker pulse is applied through C308 to the #3 grids of V304, V307, and V312, cutting off plate current flow in those tubes. This allows the grids of V305, V308, and V313 to rise from approximately -85 volts to ground potential, thus allowing V305, V308, and V313, which are the core drivers, to pulse their respective memory matrix stages and advance all the information one stage. After this, there will be new information in stage 1 and the previous digits will be in stage 2. V306 has been switched and the selectors properly reflect the condition of the memory matrix.

When V306 switched, it changed the gate tube grid voltages so that now V303B and V301A are sensitive, and V311A and V301B are not.

If a clock pulse is received at J301 (from J202), only V303B will conduct. It will switch V306 and simultaneously apply the clock pulse to grid #1 of V307, cutting it off completely. This will apply the clock pulse to V308 and pulse the corresponding memory matrix stage.

Connections to the memory stage are made directly from the driver tubes by means of plate cap connectors.

4. Memory Matrix and Read Out

The memory matrix is a modified shift register as shown in Figure XXIII. The modification consists of diodes D401, D403, D405, D410, etc. These diodes route all output pulses to the grids of the read-out tubes. However, these tubes only operate when plate voltage is applied through cathode follower V402. This, in turn, only happens when an input clock pulse cuts off V401A.

5. Pulse Peakers and Recording Drivers

The pulse peakers and recording drivers serve two purposes. When used at the output of the core matrix and read out chassis, the multivibrators are triggered by the output pulses. The multivibrator outputs at J502 are sharp-rising pulses suitable for triggering the digital-to-analog action of the decoder.

When used for recording, the pulse peakers are triggered by the output from the analog-to-digital action of the coder, and the cathode followers V502A drive the record heads, which are connected to J503.

6. Experimental Equipment

Figure XVIII shows an experimental pulse generator and record amplifier. It consists of two squaring stages V601A and V601B, intended to square up a sine wave input, triggering a variable-period one-shot multivibrator V602. The output of the multivibrator is the input to a pentode cathode follower V603 which is an easily adjustable variable current record head driver.

Figure XIX shows the experimental video amplifier. Two stages of class A amplification are followed by a high-mu triode biased below cutoff, which therefore responds only to the positive portion of the input signal.

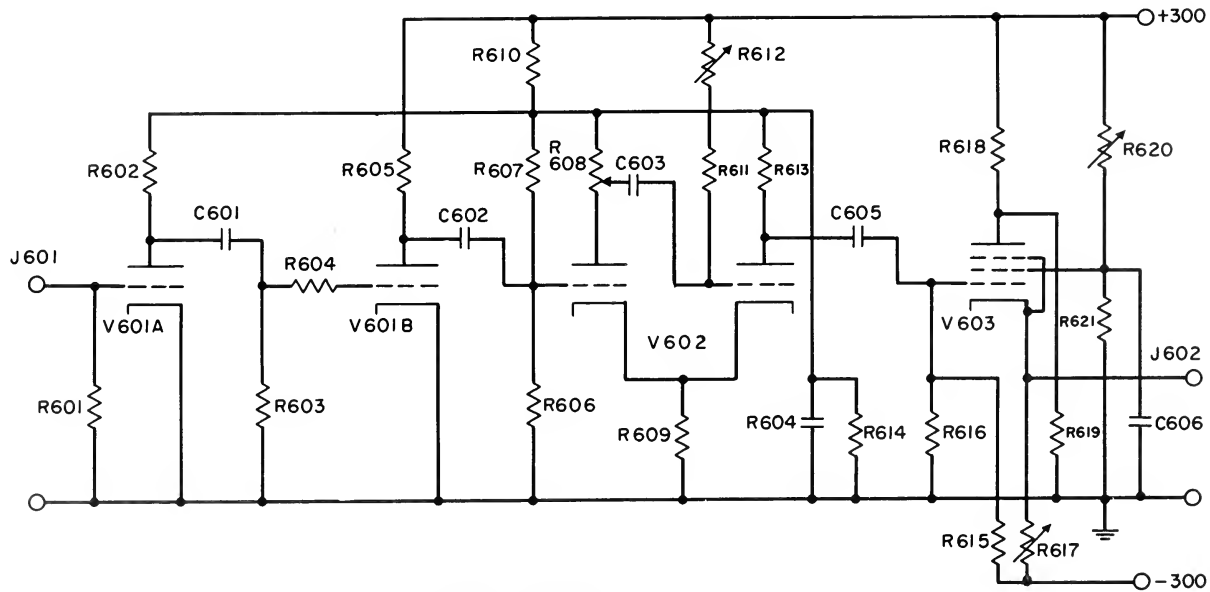


FIGURE XVIII

EXPERIMENTAL PULSE GENERATOR AND RECORD AMPLIFIER

TABLE III

Parts List for Experimental Pulse Recorder and Record Amplifier

Item	Value	Item	Value	Item	Value
R601	510K ½w	R612	2.5M 2w	C601	.001 mf
R602	51K ½w	R613	10K 2w	C602	20 mmf
R603	510K ½w	R614	51K ½w	C603	56 mmf
R604	100K ½w	R615	5.1M ½w	C604	.047 mf
R605	10K ½w	R616	1M ½w	C605	.0068 mf
R606	100K ½w	R617	See below	C606	.0068 mf
R607	510K ½w	R618	7500 10w		
R608	10K 2w	R619	2500 10w	V601	5965
R609	5K ½w	R620	See below	V602	5965
R610	12K 2w	R621	36K ½w	V603	6AK6
R611	390K ½w				

The values of R617 and R620 for various bias currents and input currents are:

	DC Bias		Tube conducting
R617	i_{head}	R620	i_{head}
37.5K	- 8 ma	105K	+16 ma
27.2K	-12 ma	63.4K	+24 ma
22.3K	-15 ma	48.2K	+30 ma
18.25K	-18 ma	40.8K	+36 ma
15.4K	-22 ma	33.0K	+42 ma

Potentiometers R608 and R612 vary the pulse length of the output of V602 from 4 microseconds to 18 microseconds.

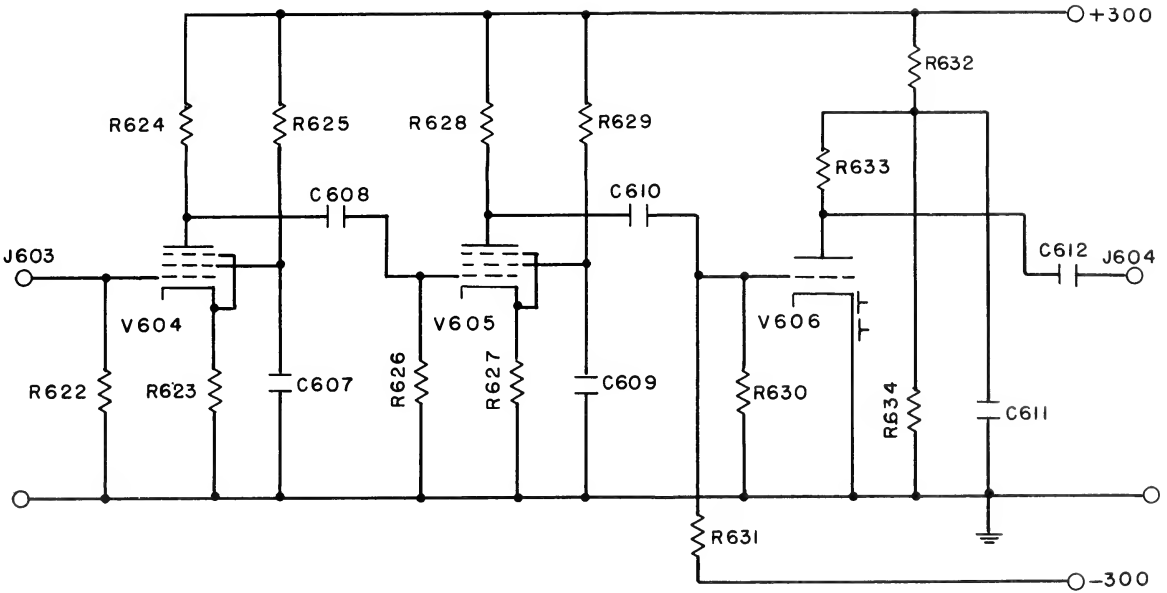


FIGURE XIX

EXPERIMENTAL VIDEO AMPLIFIER

TABLE IV

Experimental Video Amplifier

Item	Value	Item	Value
R622	1M ½w	C607	.0068 mf
R623	220 ½w	C608	.0068 mf
R624	27K 2w	C609	.0068 mf
R625	75K ½w	C610	.0068 mf
R626	470K ½w	C611	.0068 mf
R627	220 ½w	C612	.0068 mf
R628	27K 2w		
R629	75K ½w		
R630	20M ½w	V604	6AK6
R631	390K ½w	V605	6AK6
R632	15K 2w	V606	6AT6
R633	8.2K ½w		
R634	15K 2w		

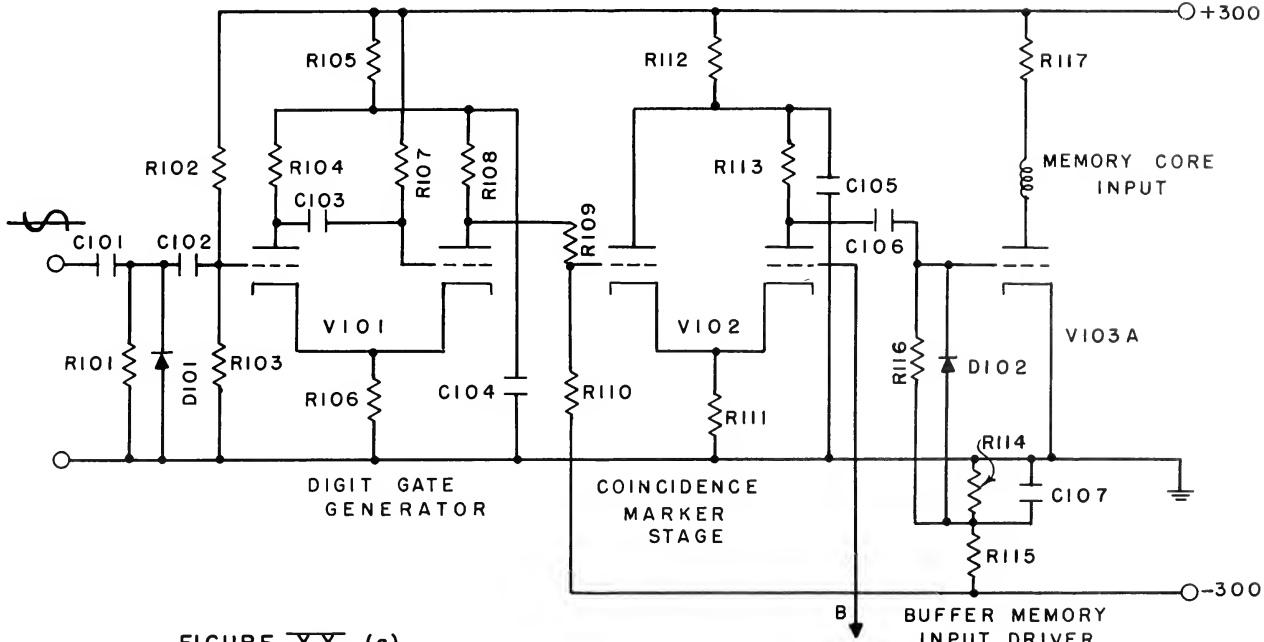


FIGURE XX (a)
SYNCHRONIZING MEMORY INPUT STAGE
(DIGITS)

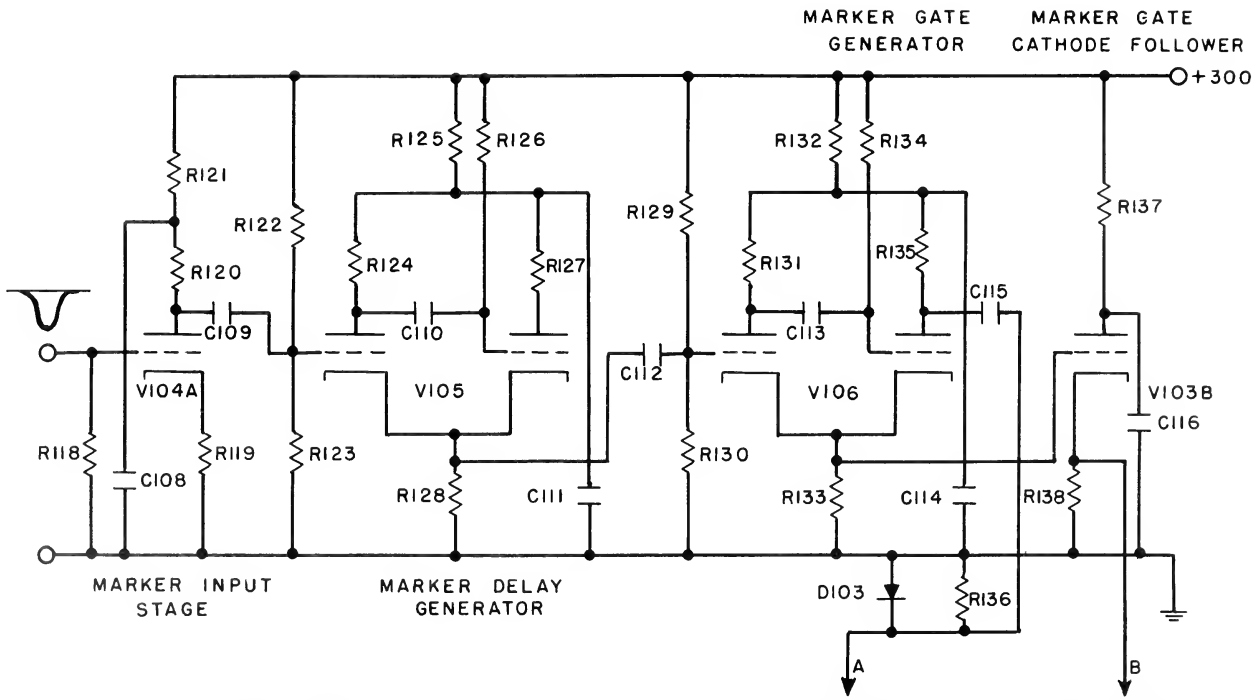


FIGURE XX (b)
SYNCHRONIZING MEMORY INPUT STAGE (MARKER)

TABLE V

Parts List for Synchronizing Memory Input Stage

Item	Value	Item	Value
R101	62K ½w	R120	10K ½w
R102	1M ½w	R121	51K ½w
R103	270K ½w	R122	1.1M ½w
R104	30K ½w	R123	51K ½w
R105	30K 1w	R124	10K ½w
R106	15K ½w	R125	15K 2w
R107	1M ½w	R126	1M ½w
R108	8.2K ½w	R127	2.2K ½w
R109	270K ½w	R128	3K ½w
R110	750K ½w	R129	1.1M ½w
R111	15K ½w	R130	51K ½w
R112	27K 2w	R131	10K ½w
R113	15K ½w	R132	15K 2w
R114	39K ½w	R133	3K ½w
R115	270K ½w	R134	1M ½w
R116	510K ½w	R135	2.2K ½w
R117	2K 2w	R136	20K ½w
R118	1M ½w	R137	4K 10w
R119	750 ½w	R138	1.2K 2 w
V101	5963	C101	.0015 mf
V102	5963	C102	150 mmf
V103	6350	C103	100 mmf
V104	5965	C104	.047 mf
V105	5963	C105	.047 mf
V106	5963	C106	470 mmf
		C107	.047 mf
D101	1N38	C108	.0062 mf
D102	1N38	C109	30 mmf
D103	1N38	C110	160 mmf
		C111	.039 mfd
		C112	30 mmf
		C113	100 mmf
		C114	.039 mf
		C115	30 mmf
		C116	3300 mmf

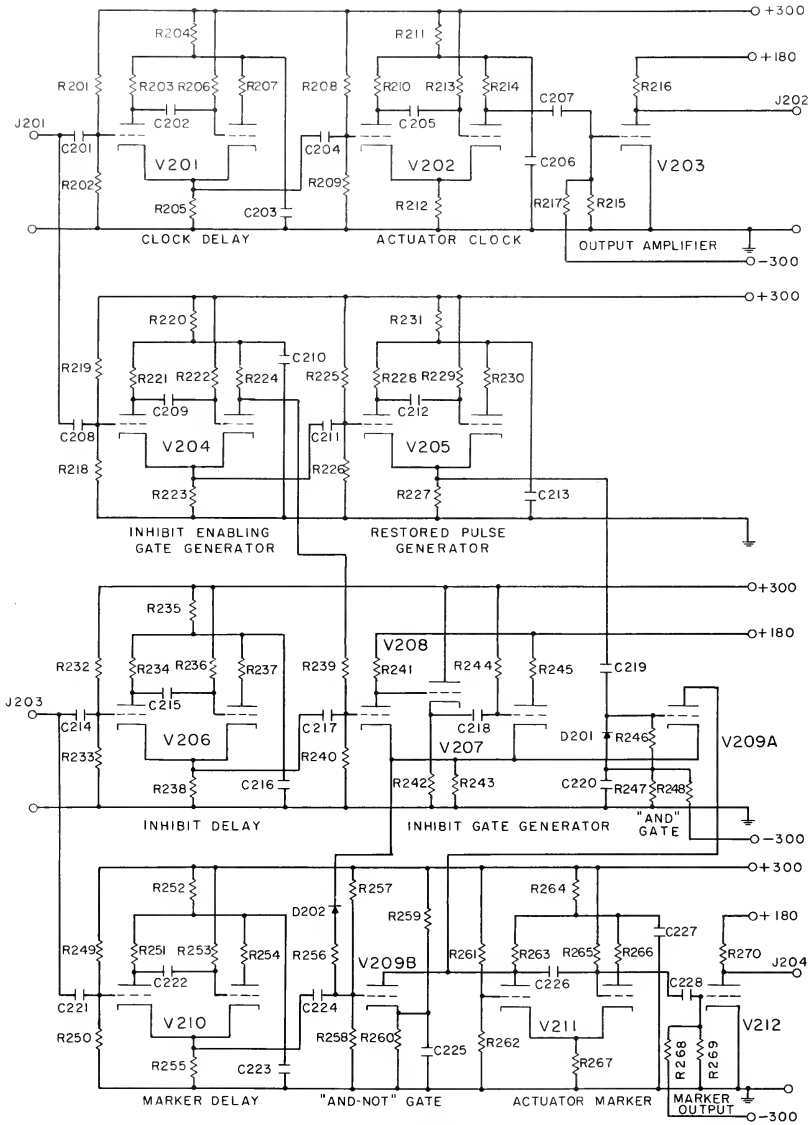


FIGURE XXI
ANTI-COINCIDENCE CIRCUIT

TABLE VI

Parts List for Anti-Coincidence Circuit

Item	Value	Item	Value	Item	Value
R201	750K ½w	R225	750K ½w	R249	620K ½w
R202	91K ½w	R226	91K ½w	R250	91K ½w
R203	10K ½w	R227	4.3K 1w	R251	10K ½w
R204	13K 2w	R228	10K ½w	R252	13K 2w
R205	4.3K 1w	R229	620K ½w	R253	1M ½w
R206	1M ½w	R230	2.2K ½w	R254	2.2K ½w
R207	2.2K ½w	R231	13K 2w	R255	4.3K 1w
R208	750K ½w	R232	620K ½w	R256	10K ½w
R209	91K ½w	R233	75K ½w	R257	680K ½w
R210	10K ½w	R234	10K ½w	R258	100K ½w
R211	13K 2w	R235	13K 2w	R259	270K ½w
R212	4.3K 1w	R236	820K ½w	R260	51K ½w
R213	390K ½w	R237	2.2K ½w	R261	560K ½w
R214	2.2K ½w	R238	4.3K 1w	R262	91K ½w
R215	100K ½w	R239	240K ½w	R263	10K ½w
R216	1.5K ½w	R240	75K ½w	R264	13K 2w
R217	1.5M ½w	R241	270K ½w	R265	390K ½w
R218	91K ½w	R242	39K 1w	R266	2.2K ½w
R219	750K ½w	R243	5.6K 1w	R267	4.3K 1w
R220	13K 2w	R244	5.1M ½w	R268	1.5M ½w
R221	10K ½w	R245	3K ½w	R269	100K ½w
R222	1M ½w	R246	100K ½w	R270	1.5K ½w
R223	4.3K 1w	R247	100K ½w		
R224	6.2K ½w	R248	omit		
C201	33 mmf	C215	56 mmf	V201	5963
C202	224 mmf	C216	.01 mf	V202	5965
C203	.0068 mf	C217	15 mmf	V203	6C4
C204	18 mmf	C218	47 mmf	V204	5965
C205	27 mmf	C219	18 mmf	V205	5965
C206	.01 mf	C220	.001 mf	V206	5963
C207	470 mmf	C221	10 mmf	V207	5965
C208	22 mmf	C222	89 mmf	V208	6C4
C209	220 mmf	C223	.01 mf	V209	5965
C210	.01 mf	C224	33 mmf	V210	5963
C211	10 mmf	C225	470 mmf	V211	5965
C212	93 mmf	C226	27 mmf	V212	6C4
C213	.01 mf	C227	.01 mf		
C214	55 mmf	C228	470 mmf	D201	1N38
				D202	1N38

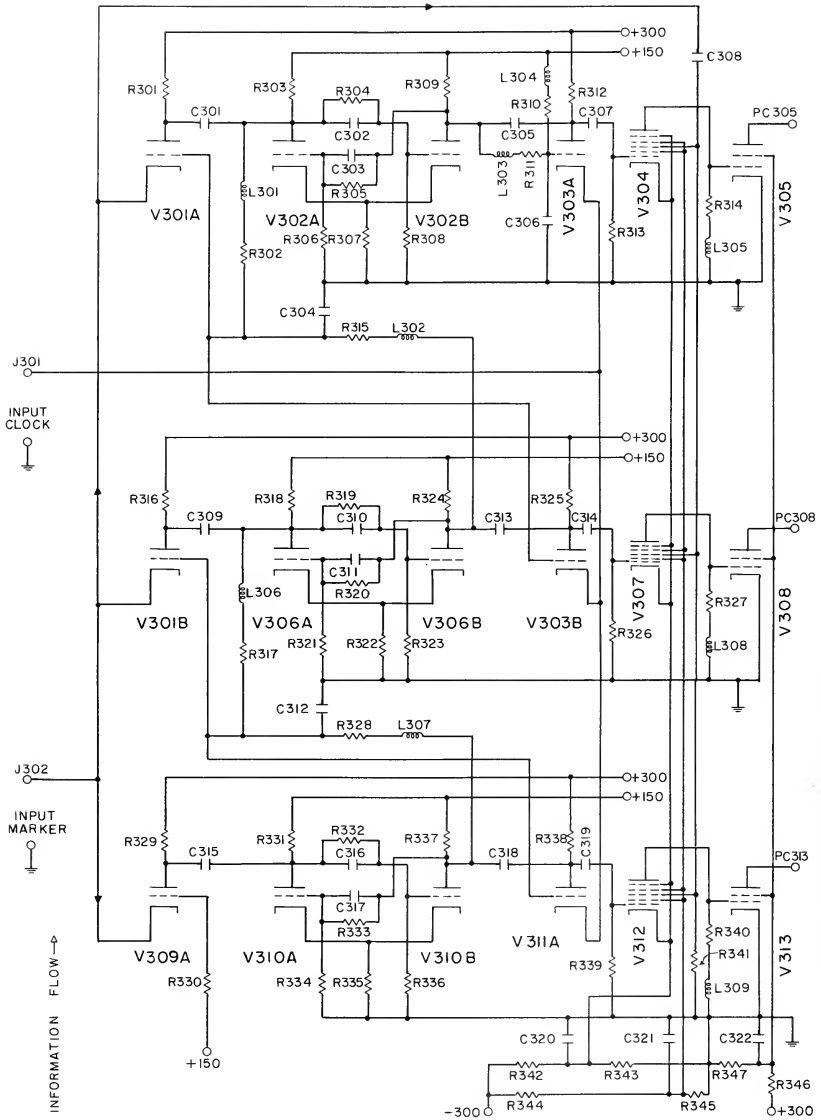


FIGURE XXII
SCHEMATIC- READ-OUT SELECTORS

TABLE VII

Parts List for Read-out Selectors

Item	Value	Item	Value	Item	Value
R301	33K ½w	R317	100K ½w	R333	510K ½w
R302	100K ½w	R318	7.5 ½w	R334	270K ½w
R303	7.5K ½w	R319	510K ½w	R335	6.8K ½w
R304	510K ½w	R320	510K ½w	R336	270K ½w
R305	510K ½w	R321	270K ½w	R337	7.5K ½w
R306	270K ½w	R322	6.8K ½w	R338	33K ½w
R307	6.8K ½w	R323	270K ½w	R339	1M ½w
R308	270K ½w	R324	7.5K ½w	R340	15K ½w
R309	7.5K ½w	R325	33K ½w	R341	1M ½w
R310	100K ½w	R326	1M ½w	R342	7K 10w
R311	100K ½w	R327	15K ½w	R343	omit
R312	33K ½w	R328	100K ½w	R344	omit
R313	1M ½w	R329	33K ½w	R345	4K 2w
R314	15K ½w	R330	100K ½w	R346	4K 10w
R315	100K ½w	R331	7.5K ½w	R347	12.5K 10w
R316	33K ½w	R332	510K ½w		
C301	100 mmf	C312	5 mmf	V301	5963
C302	10 mmf	C313	22 mmf	V302	5965
C303	10 mmf	C314	15 mmf	V303	5963
C304	5 mmf	C315	100 mmf	V304	5915
C305	37 mmf	C316	10 mmf	V305	6146
C306	10 mmf	C317	10 mmf	V306	5965
C307	15 mmf	C318	22 mmf	V307	5915
C308	68 mmf	C319	15 mmf	V308	6146
C309	100 mmf	C320	.5 mfd	V309	5963
C310	10 mmf	C321	.1 mfd	V310	5965
C311	10 mmf	C322	.1 mfd	V311	5963
				V312	5915
L301	100 mh	L305	5 mh	V313	6146
L302	100 mh	L306	100 mh		
L303	100 mh	L307	100 mh		
L304	100 mh	L308	5 mh		
		L309	5 mh		

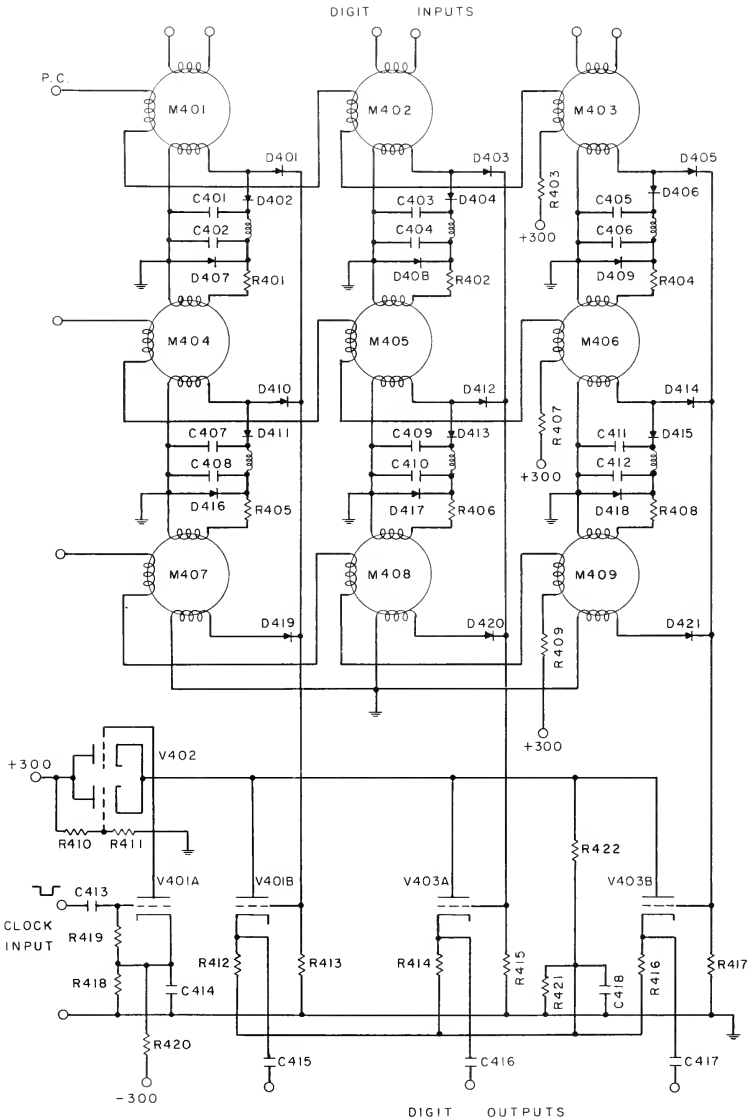


FIGURE XXIII

CORE MATRIX AND READ-OUT GATES

TABLE VIII

Parts List for Core Matrix and Read Out

Item	Value
R401	Part of M401
R402	Part of M402
R403	51 2w
R404	Part of M403
R405	Part of M404
R406	Part of M405
R407	51 2w
R408	Part of M406
R409	51 2w
R410	150K ½w
R411	75K ½w
R412	10K ½w
R413	51K ½w
R414	10K ½w
R415	51K ½w
R416	10K ½w
R417	51K ½w
R418	13K ½w
R419	470K ½w
R420	43K 2w
R421	3.3K ½w
R422	120K 1w
M401	Epsco SR-200C
M402	Epsco SR-200C
M403	Epsco SR-200C
M404	Epsco SR-200C
M405	Epsco SR-200C
M406	Epsco SR-200C
M407	Epsco SR-200C
M408	Epsco SR-200C
M409	Epsco SR-200C
V401	5965
V402	6350
V403	5965

Item	Value
C401	Part of M401
C402	Part of M401
C403	Part of M402
C404	Part of M402
C405	Part of M403
C406	Part of M403
C407	Part of M404
C408	Part of M404
C409	Part of M405
C410	Part of M405
C411	Part of M406
C412	Part of M406
C413	100 mmf
C414	.01 mf
C415	.001 mf
C416	.001 mf
C417	.001 mf
C418	.01 mf
D401	1N38
D402	T6G
D403	1N38
D404	T6G
D405	1N38
D406	T6G
D407	T6G
D408	T6G
D409	T6G
D410	1N38
D411	T6G
D412	1N38
D413	T6G
D414	1N38
D415	T6G
D416	T6G
D417	T6G
D418	T6G
D419	1N38
D420	1N38
D421	1N38

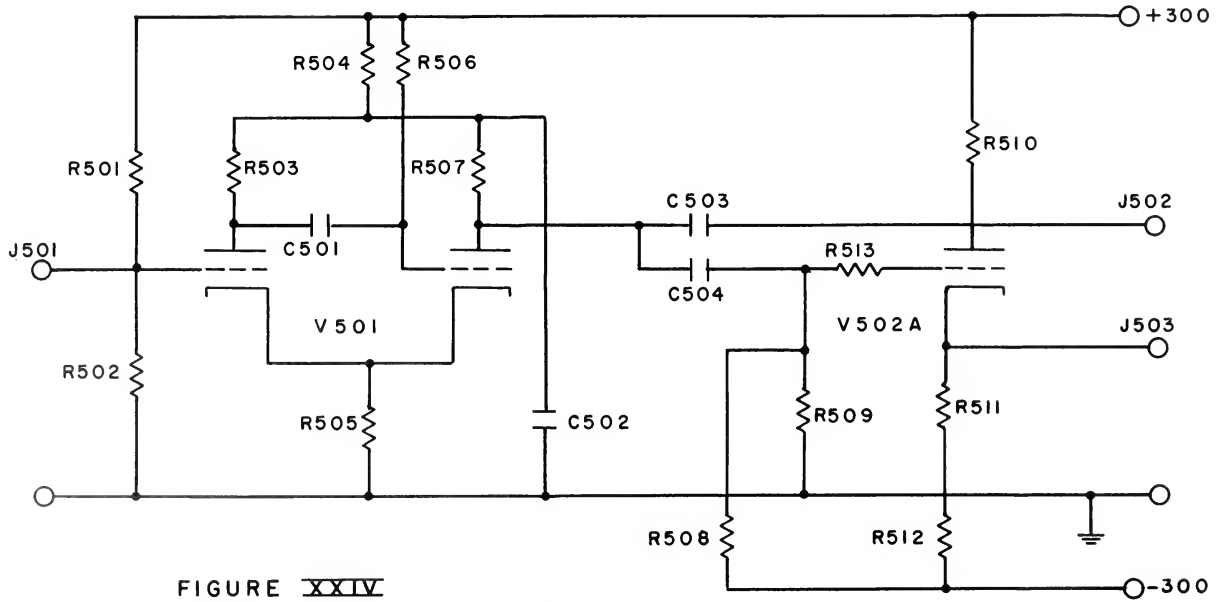


FIGURE XXIV

PULSE PEAKERS AND RECORD AMPLIFIERS

TABLE IX

Parts List for Pulse Peakers and Record Amplifiers

Item	Value	Item	Value
R501	680K ½w	C501	130 mmf.
R502	100K ½w	C502	.01 mf
R503	16K ½w	C503	100 mmf
R504	2.2K 2w	C504	.0068 mf
R505	6.8K 1w		
R506	750K ½w	V501	5965
R507	8.2K 1w	V502	6350
R508	470K ½w		
R509	100K ½w		
R510	3.6K 2w		
R511	15K 2w		
R512	15K 2w		
R513	100K ½w		

APPENDIX C

Specifications of the Magnetic Storage Element SR 200C Made by Epsco, Incorporated, Boston, Massachusetts [5]

1) Information Rate Design Center . . . . . 200 KC

2) Practical Upper Information Rate . . . . 350 KC

3) Maximum peak power per shifted one at design center: . . . 2.0 watts

4) Cores per binary digit 1

5) Cores shall be capable of shifting with a drive current whose amplitude is 400 ma or less and whose pulse width is between .8 and 1.2 micro-seconds

6) Minimum signal output voltage loaded with next core input winding: . . . . . 10 volts

7) Maximum voltage drop across drive winding at 400 ma. . . . . 6 volts

8) Units to be used with Transitron Type T6G diode or exact equivalent or Hughes #D2172, #D2162

9) Peak inverse voltage diode rating minimum . 20 volts

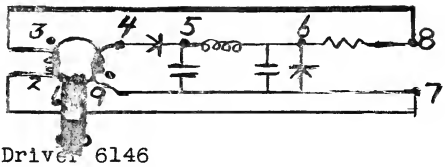
10) Read-in requirements: . . . . . 20 volts DC-3 ma.

10 sec pulse
20 ma (2V)

5 sec pulse
40 ma (4V)

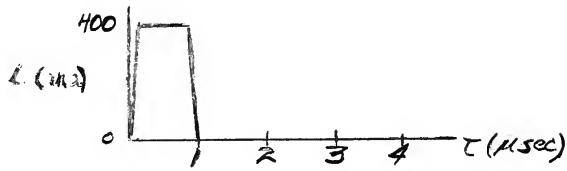
11) Breakdown between windings shall not occur for DC voltage differences of less than 300V. Test voltage 600V.

a) Circuit Diagram

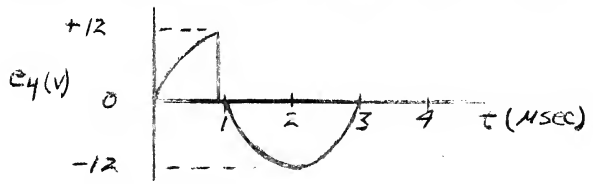


Driver 6146

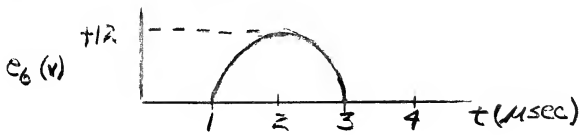
b) Drive Pulse at Terminal 9



c) Read-out followed by one read-out from previous stage



d) Read-out at Terminal 6



e) Drive current vs. Pulse Length

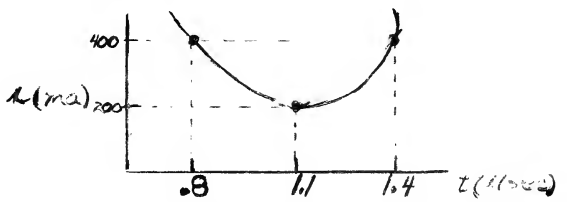


Figure XXV

Performance Curves - Epsco SR 200C

Appendix D

Photographs of System Components

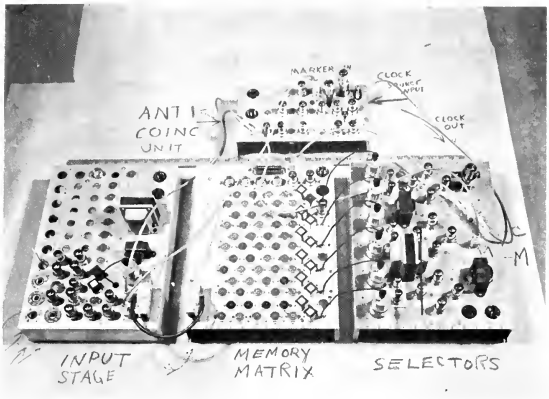


Figure XXVI(a)
Complete System with Signal Cables

Figure XXVI(b)
Ampex Model 307, 7 channel recorder

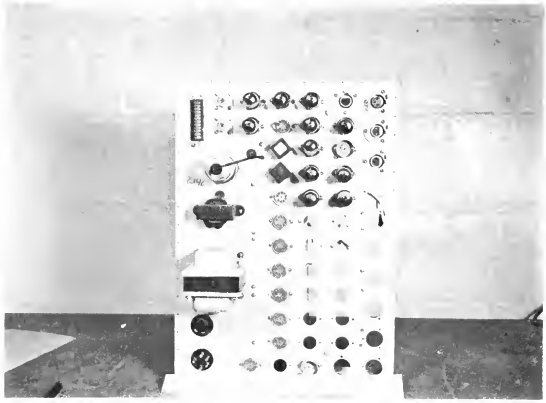


Figure XXVII(a)
Synchronizing Memory Input
Stage

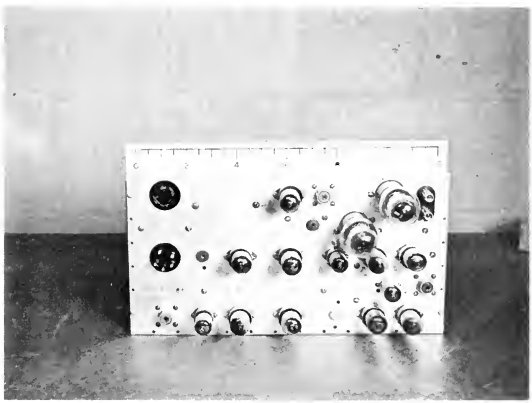


Figure XXVII(b)
Anti-Coincidence Circuit

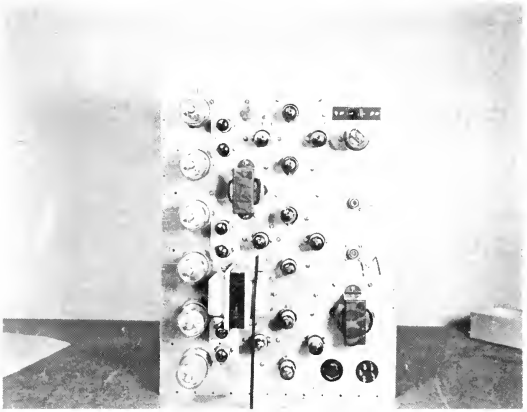


Figure XXVIII(a)
Read-out Selectors, front

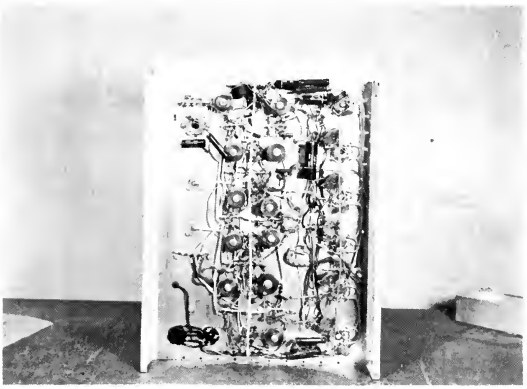


Figure XXVIII(b)
Read-out Selectors, back

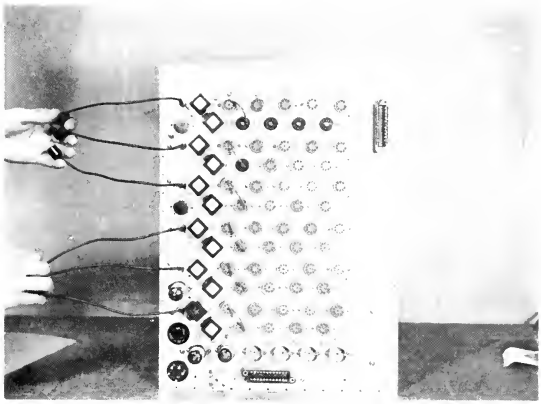


Figure XXIX(a)
Memory Matrix
Note plate caps for 6146s

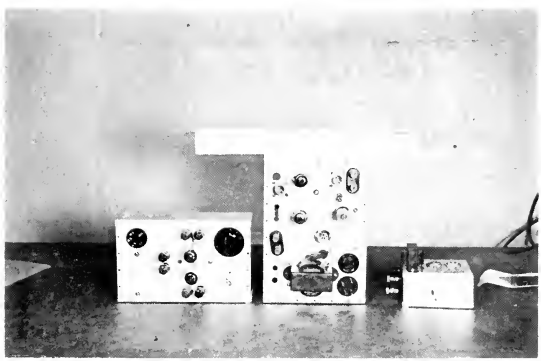


Figure XXIX(b)
Test Equipment
Program gen. Video amp. Pulse gen.

APPENDIX E

Literature Citations

1. "Flutter-free Magnetic Recording," Hitt, J. J., E. E. Thesis MIT-1952.

2. "Flutter in Magnetic Tape Recording," Prager, R. H., E. E. Thesis MIT- 1952.

3. Instruction book for Model 307 Magnetic Tape Recorder Ampex Electric Corporation, 934 Charter St., Redwood City, California.

4. Probability and Information Theory , Woodward, P. M. McGraw-Hill Book Co., Inc., New York, 1955

5. Epsco, Incorporated. 588 Commonwealth Ave., Boston, Massachusetts